ADQ14 Datasheet

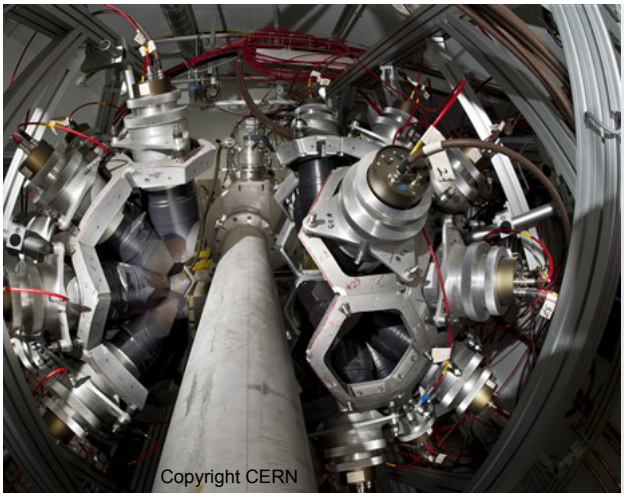
ADQ14 is a versatile 14-bit high-end data acquisition platform, designed to meet the most challenging measurement situations. ADQ14 features:

1 to 4 channels and multi-board sync

500 MSPS up to 2 GSPS per channel

3.2 GByte/s data transfer rate

Open FPGA for real-time DSP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ADQ14 Datasheet

Features

- Up to 4 analog channels
- Up to 2 GSPS sample rate per channel
- 14 bits vertical resolution
- DC-coupled with up to 1.2 GHz analog BW
- AC-coupled with up to 1.2 GHz analog BW
- Programmable DC-offset
- Internal and external clock reference
- Internal and external clock generator
- Clock reference output
- Internal and external trigger
- Trigger output
- Multi-channel synchronization
- Time-stamp for real-time operation
- 2 GBytes data memory
- Data interface PXIe / PCIe / USB3.0 / MTCA.4

ADQ14 Development Kit

- Open FPGA for custom applications
- Real-time signal processing

Applications

- RADAR
- LIDAR
- Wireless communication
- High-speed data recording
- Test and measurement
- Ultrasonic ranging
- Time-of-flight
- Thomson scattering

Advantages

- Host PC form factor options for optimized systems partitioning.
- Analog front-end options for meeting sensor and measurement requirements.
- Sample rate options that supports a wide range of products and streamlined maintenance. This optimizes cost of ownership.
- Real-time custom processing solutions for advanced systems.
- SP Devices' design service is available for fast integration to lower time-to-market.

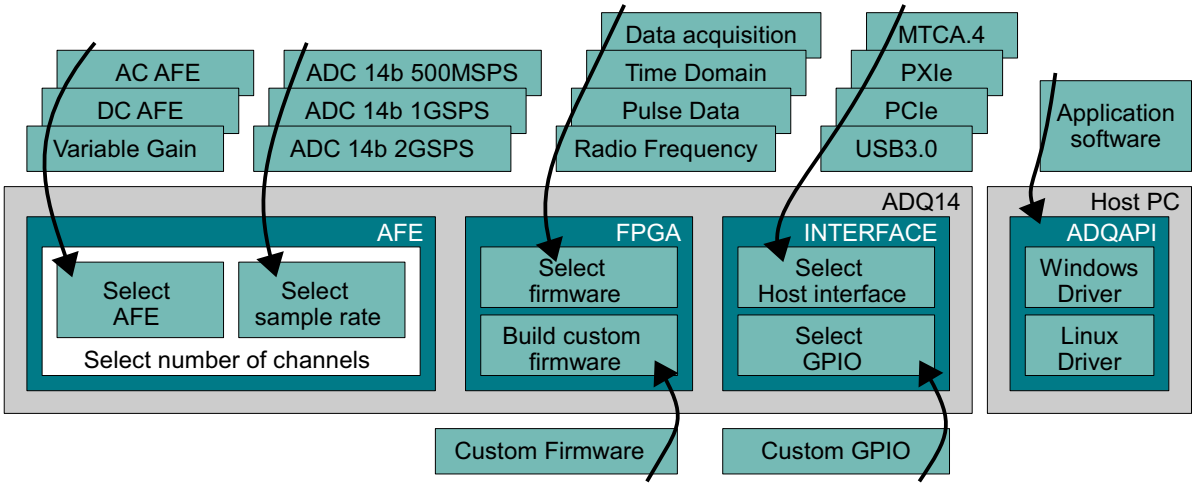
Flexible digitizer solution

Configure the ADQ14 to meet the measurement challenge. Select DC- or AC-coupled front-end and sampling rate. The DC-coupled front-end is also available with variable gain. Select the number of channels between 1 and 4. Further expansion is possible by synchronizing several ADQ14.

There are several firmware options for typical measurement situations. Custom firmware is enabled through the open FPGA architecture.

Select the host interface for optimal systems design. The form factor sets the communication interface to the host PC as well as the mechanical properties of the ADQ14.

The software development kit is used for implementing the controlling application. It is available for Windows and the main Linux distributions.



1 Selection guide

There are several options for ADQ14. This guide will help you through the selection of options. Follow the procedure listed to select the features. Please use the table below to see which combinations that are available. Each of the items below are described further later in the document.

1. Select AC- or DC-coupled front-end. This will give the model ADQ14AC or ADQ14DC.
2. Select the number of channels and the sample rate; –2A, –2C, –1X, –4A, –4C or –2X.
3. Select variable input range option; –VG.
4. Select host interface; –USB, –PXIE, –PCIE or –MTCA.
5. Select one or several of the firmware packages; –FWDAQ, –FWATD, –FWPD or –FWSDR.
6. Select GPIO front panel connector option; –GPIO.
7. Add ADQ14 Development Kit for custom real-time signal processing in the FPGA.

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Key parameters												
Number of channels	2	2	1	4	4	2	2	2	1	4	4	2
Sample rate / channel [GSPS]	0.5	1	2	0.5	1	2	0.5	1	2	0.5	1	2
Analog front-end (Factory installed)												
AC-Coupling	✓	✓	✓	✓	✓	✓						
DC-Coupling							✓	✓	✓	✓	✓	✓
50 Ω input impedance	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Variable DC-offset	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Variable input range[1 2] –VG							✓	✓	✓	✓	✓	✓
Overvoltage protection	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Anti-aliasing filter							✓	✓	✓	✓	✓	✓
Firmware												
ADQ14 Development Kit	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Acquisition[3] –FWDAQ	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Adv. time domain –FWATD	✓	✓	✓	_[4]	_[4]	_[4]	✓	✓	✓	_[4]	_[4]	_[4]
Pulse data –FWPD		✓		✓	✓	✓		✓		✓	✓	✓
Radio Systems –FWSDR	✓	✓		✓	✓	✓	✓	✓		✓	✓	✓
Synchronization												
External clock/clock ref	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
External trigger in/out	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Multi-unit synchronization[5]				✓	✓	✓				✓	✓	✓
Host interface												
USB3 –USB	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCIe Gen2 x8 –PCIE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PXIe Gen2 x8 –PXIE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M-TCA.4[2 6] –MTCA											✓	✓
12 pins GPIO[1 6] –GPIO	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

1. The –GPIO option is included with the variable gain option, –VG.
2. The –VG option is not available for –MTCA form factor.
3. Included with the ADQ14.
4. Contact SP Devices
5. Requires firmware option –FWPD.
6. The –GPIO option is available as standard on the –MTCA form factor.

2 Technical data[1]

Table 1: General parameters

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Key parameters												
Channels	2	2	1	4	4	2	2	2	1	4	4	2
Sample rate / channel [GSPS]	0.5	1	2	0.5	1	2	0.5	1	2	0.5	1	2
Resolution [bits]	14						14					
Data memory[1] [GByte]	2						2					
Power												
Power supply [V]	12						12					
Power dissipation [W]	36	36	36	42	42	42	39	39	39	48	48	48

1. The data memory is shared between data (2 bytes per sample) and record headers.

Table 2: Analog input

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Analog inputs												
Coupling	AC						DC					
Input Impedance AC [Ω]	50						50					
Input Impedance DC [Ω]	100k						50					
Input range [V_{pp}]	1.9						0.5	0.5	1	0.5	0.5	1
Bandwidth lower –3 dB [Hz]	80	80	100	80	80	100	DC					
Bandwidth upper –1 dB [MHz]	900	900	800	900	900	800	180	500	900	180	500	900
Bandwidth upper –3 dB [MHz]	1200	1200	1000	1200	1200	1000	250	700	1200	250	700	1200
Connector	SMA						SMA					
Variable gain –VG option												
Input range 0.2 Vpp	–						✓	✓	–	✓	✓	–
Input range 0.5, 1, 2, 5 Vpp	–						✓	✓	✓	✓	✓	✓
Bandwidth –1 dB –VG[1] [MHz]	–						180	400	700	180	400	700
Bandwidth –1 dB –VG[2] [MHz]	–						180	300	450	180	300	450
Bandwidth –3 dB –VG[1] [MHz]	–						250	500	900	250	500	900
Bandwidth –3 dB –VG[2] [MHz]	–						250	400	700	250	400	700
Variable DC-offset												
Variable DC-offset range[3] [V]	±1.05						±0.25					
Variable DC-offset steps	31						31					

1. Ranges 0.2 Vpp 0.5 Vpp.
2. Ranges 1 Vpp, 2 Vpp and 5 Vpp.
3. The variable DC-offset covers the full scale of the signal. For the –VG option, the full range of each respective range setting is covered by the variable DC-offset.

1. All values are typical unless otherwise noted.

Table 3: Over-voltage protection

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Overvoltage protection												
Max input voltage [V]	–						±5		–	±5		–
Max input current [mA]	±100						–		±100	–		±100
–VG range 0.2 V_{pp} [V]	–						±4		–	±4		–
–VG range 0.2 V_{pp} [mA]	–						–		±100	–		±100
–VG option other ranges [V]	–						±5					

Table 4: Dynamic performance[1]

MODEL	ADQ14AC[2] (TBC)						ADQ14DC[3]					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Analog performance with overvoltage protection activated												
SNR [dB]	64	64	64	64	64	64	62	60	58	62	60	58
SNDR [dB]	59	59	59	59	59	59	62	60	58	62	60	58
SFDR [dBc]	61	61	61	61	61	61	75	75	75	75	75	75
ENOB [bits]	9.6	9.6	9.6	9.6	9.6	9.6	10	9.7	9.3	10	9.7	9.3
Analog performance without overvoltage protection												
SNR [dB]	64	64	64	64	64	64	–					
SNDR [dB]	63	63	63	63	63	63	–					
SFDR [dBc]	69	69	69	69	69	69	–					
ENOB [bits]	10.2	10.2	10.2	10.2	10.2	10.2	–					
Analog performance –VG option range 0.5 1 2 5 Vpp												
ENOB [bits]	–						10	9.7	9.3	10	9.7	9.3
SFDR [dBc]	–						75	75	75	75	75	75
Analog performance –VG option range 0.2 Vpp												
ENOB [bits]	–						9.4	9.1	–	9.4	9.1	–
SFDR [dBc]	–						75	75	–	75	75	–

1. All values are preliminary
2. At 71 MHz -1dBFS input signal.
3. At 71 MHz -1dBFS input signal.

Table 5: Clock

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Internal Clock Reference												
Frequency [MHz]	10						10					
Accuracy [ppm]	± 3 ± 1/year						± 3 ± 1/year					
External clock reference input												
Frequency (min – max) [MHz]	10 MHz ± 5 ppm						10 MHz ± 5 ppm					
Signal level (min – max) [Vpp]	0.5 – 3.3						0.5 – 3.3					
Impedance AC [Ω]	50						50					
Impedance AC (high[1]) [Ω]	200						200					
Impedance DC [Ω]	10 k						10 k					
Duty cycle	TBD						TBD					
Connector	SMA						SMA					
PXIe clock reference[2]												
PXIe clock [MHz]	100						100					
PXIe sync[3] [MHz]	10						10					
Clock reference output												
Frequency [MHz]	Set by selected clock reference						Set by selected clock reference					
Signal level [Vpp]	1.2 (into 50 Ω load)						1.2 (into 50 Ω load)					
Impedance AC [Ω]	50						50					
Impedance DC [Ω]	10 k						10 k					
Duty cycle	50% ± 5%						50% ± 5%					
Connector	SMA						SMA					
External clock source												
Frequency [GHz]	1						1					

1. Software-controlled high-impedance setting for large fan-out situations.
2. Available on ADQ14 with option –PXIE in a chassis that supports PXIe.
3. Jitter of PXIe sync is reduced by PXIe clock in the ADQ14.

Table 6: Trigger

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
External trigger input												
Trigger frequency (max) [MHz]	>1						>1					
Signal level (min – max) [V]	–0.5 to 3.3						–0.5 to 3.3					
Threshold[1] [V]	Programmable						Programmable					
Sensitivity [mV]	200						200					
Time resolution [ps]	125						125					
Excess jitter[2] [ps]	25						25					
Impedance DC [Ω]	50						50					
Impedance DC (high[3]) [Ω]	>500						>500					
GPIO data rate[4] [MHz]	125						125					
Connector	SMA						SMA					
Trigger output												
PRF (max) [MHz]	100						100					
Signal level output low max [V]	0.1						0.1					
Signal level output high min [V]	1.2 (into 50 Ω load)						1.2 (into 50 Ω load)					
Impedance DC [Ω]	50						50					
GPIO data rate[4] [MHz]	TBD						TBD					
Connector	Shared with trigger input						Shared with trigger input					

1. Set threshold to match requested electrical standard when operated as GPIO input.
2. The trigger is synchronous to the sampling and can be resolved with sub-sample precision. The excess jitter is jitter added to the trigger signal inside the ADQ14.
3. Software-controlled high-impedance setting for large fan-out situations.
4. When used as GPIO.

Table 7: Multi-Unit Synchronization

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
External sync input												
PRF (max) [MHz]	>1						>1					
Signal level input low max [V]	0.8						0.8					
Signal level input high min [V]	2						2					
Impedance DC [Ω]	50						50					
Impedance DC (high[1]) [Ω]	>500						>500					
GPIO data rate [MHz]	100						100					
Connector (–PCIE)	MCX inside PC chassis						MCX inside PC chassis					
Connector (other form factor)	SMA shared with Sync out						SMA shared with Sync out					
Sync output												
PRF (max) [MHz]	>1						>1					
Signal level output low max [V]	0.1						0.1					
Signal level output high min [V]	1.2 (into 50 Ω load)						1.2 (into 50 Ω load)					
Impedance DC [Ω]	50						50					
GPIO data rate [MHz]	100						100					
Connector (–PCIE)	MCX inside PC chassis						MCX inside PC chassis					
Connector (other form factor)	SMA shared with Sync input						SMA shared with Sync input					

1. Software-controlled high-impedance setting for large fan-out situations.

Table 8: GPIO

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Standard GPIO												
Trigger input/output	See trigger specification						See trigger specification					
Sync input/output	See sync specification						See sync specification					
GPIO option –GPIO (Included with the –VG, variable gain option)												
Number of GPIO signals	12						12					
Signal level input high min [V]	0.8						0.8					
Signal level input low max [V]	2						2					
Input impedance [Ω]	10k						10k					
Signal level output low max [V]	0.1 (no load)						0.1 (no load)					
Signal level output high min [V]	3.1 (no load)						3.1 (no load)					
Output impedance [Ω]	90						90					
Max data rate [Mbit/s per pin]	100						100					
GPIO power out [V]	3.3						3.3					
GPIO power out [mA]	100						100					
Connector	Hirose ST60-24P(50)											
Cable	See ordering information											

Table 9: Environment

INTERFACE TO HOST PC	USB3.0	PCI EXPRESS	PXI EXPRESS
OPTION	–USB	–PCIE	–PXIE
Data rate			
Standard	USB3.0	Gen2 by 8 lanes	Gen2 by 8 lanes
Data rate sustained[1] [MBytes/s]	200	3200[2]	3200[2]
Mechanical			
Box size [mm^3]	191 x 108 x 62	–	–
Weight [g]	750	–	–
Bus width mechanical [lanes]	–	16[3]	8
Board width (ADQ14AC) [slot]	–	2	1 slot 4TE
Board width (ADQ14DC) [slot]	–	2	2 slot 8TE
Board length	–	short	160 mm
Board height	–		3U
Electrical			
Power supply	External[4]	6-pin ATX power	From chassis
Bus width electrical [lanes]	–	8	8
Temperature range			
Operation [^{o}C]	0 to 45	0 to 45	0 to 45 [5]
Compliances			
CE	✓	✓	✓
RoHS2	✓	✓	✓

1. This is depending on the capacity of the complete system including the host computer.
2. On 8 lanes.
3. The wide contact is required to support the weight of the board.
4. Use only the power supply which is included in the delivery of ADQ14–USB.
5. High fan setting required if available on the chassis.

Table 10: Firmware options functions overview

MODEL / OPTION	ADQ14AC –FWDAQ	–FWATD	–FWPD	–FWSDR	
Trigger modes					
Software trigger	✓	✓		✓	
External trigger	✓	✓		✓	
Common level trigger	✓[1]				
Individual level trigger			✓[2]		
PXIe backplane trigger[3]	✓			✓	
Internal trigger	✓	✓		✓	
Trigger output					
Internal trigger []	✓	✓	✓	✓	
Trigger event	✓	✓	✓	✓	
Clock					
All clock modes	✓	✓	✓	✓	
Sample skip	✓			✓	
Multi-unit sync			✓		
Data acquisition modes					
Continuous streaming	✓			✓	
Triggered streaming w header	✓	✓	✓	✓	
Triggered streaming w/o header	✓			✓	
Multi-record	✓			✓	

1. All channel trigger on one selected channel.
2. Each channel trigger independently of the others.
3. Requires –PXIE option in a chassis with PXIe trigger support.

Table 11: Data acquisition parameters

MODEL		ADQ14AC AND ADQ14DC					
OPTION		–2A	–2C	–1X	–4A	–4C	–2X
Triggered streaming							
Re-arm time	[ns]	8	8	16	8	8	16
Pre-trigger	[samples]	16 ki	16 ki	16 ki	16 ki	16 ki	16 ki
Pre-trigger step	[samples]	4	4	8	4	4	8
Trigger delay	[samples]	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$
Trigger delay step	[samples]	4	4	8	4	4	8
Record length max	[samples]	2 Gi	2 Gi	2 Gi	2 Gi	2 Gi	2 Gi
Record length min	[samples]	8	8	16	8	8	16
Record length step	[samples]	1	1	1	1	1	1
Multi-record							
Re-arm time	[ns]	TBD	TBD	TBD	TBD	TBD	TBD
Pre-trigger	[samples]	Record length					
Pre-trigger step	[samples]	4	4	8	4	4	8
Trigger delay	[samples]	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$
Trigger delay step	[samples]	4	4	8	4	4	8
Record length max	[samples]	500 Mi	500 Mi	1000 Mi	250 Mi	250 Mi	500 Mi
Record length min	[samples]	TBD	TBD	TBD	TBD	TBD	TBD
Record length step	[samples]	TBD	TBD	TBD	TBD	TBD	TBD
Continuous streaming							
Data rate		PC link speed limit					

Table 12: Software support

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Operating systems												
Windows 7 32b and 64b	✓						✓					
Windows 8 / 8.1	✓						✓					
Windows 10	✓						✓					
Linux[1]	Kernel 2 and 3, main distributions						Kernel 2 and 3, main distributions					
Application												
ADCaptureLab[2]	Acquisition and analysis						Acquisition and analysis					
MATLAB[2]	API, examples						API, examples					
C/C++	API, examples						API, examples					
.Net (C#, Visual Basic)	API, examples						API, examples					
Python	Example scripts						Example scripts					
LabVIEW	DLL import						DLL import					

1. Contact an SP Devices sales representative for information about currently supported distributions.
2. Windows only.

3 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device.

The ADQ14–USB and ADQ14–PCIE has a built-in fan to cool the device. ADQ14–PXIE is cooled from the chassis fan. The built-in temperature monitoring unit will protect the ADQ14 from over-heating by temporarily shutting down parts of the device in an overheat situation.

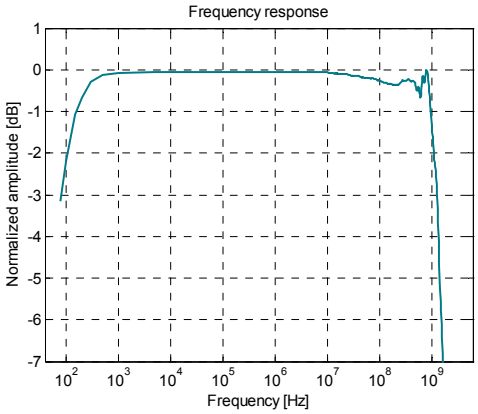
The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are required.

Table 13: Absolute Maximum Ratings

MODEL		ADQ14AC						ADQ14DC					
OPTION		–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Analog input													
AC (with ovp)		See Table 3						See Table 3					
AC w/o ovp f >10 MHz	[Vpp]	5						TBD					
AC w/o ovp f <10 MHz	[Vpp]	2.75						TBD					
DC max[1]	[V]	+7						See Table 3					
DC min[1]	[V]	–3						See Table 3					
External clock reference													
Signal level AC	[Vpp]	5						5					
Signal level DC	[V]	± 5						± 5					
External trigger input													
Signal level to GND min	[V]	–2.3						–2.3					
Signal level to GND max	[V]	+5						+5					
External sync input													
Signal level to GND min	[V]	–0.5						–0.5					
Signal level to GND max	[V]	+3.8						+3.8					
Power supply													
Voltage to GND (min)	[V]	–0.4						–0.4					
Voltage to GND (max)	[V]	14						14					
Temperature													
Operating (min)	[^{o}C]	0						0					
Operating (max)	[^{o}C]	45						45					
Standard GPIO													
Trigger input		Se trigger specification						Se trigger specification					
Sync		Se sync specification						Se sync specification					
GPIO Expansion –GPIO													
Voltage to GND (min)	[V]	–0.5						–0.5					
Voltage to GND (max)[2]	[V]	4.6						4.6					
Max output current per pin	[mA]	33						33					
Max total output current	[mA]	200						200					
Variable gain –VG													
Relay switching cycles		N/A						10^{6}					

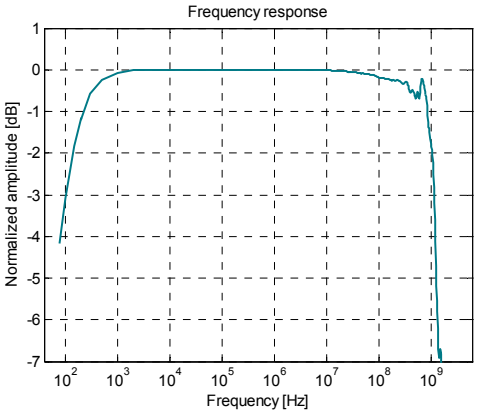
1. The combination of AC and DC level must never exceed DC level limits.
2. A voltage on a GPIO input higher than 3.3 V may change the output voltage on GPIOs which are set to outputs. This may damage external equipment.

4 Frequency response[1]



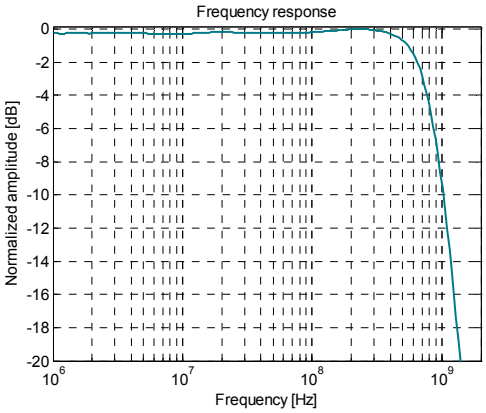
Bandwidth (–3 dB)	1200 MHz
1 dB flatness	900 MHz

Figure 1: ADQ14AC–4C (TBC)



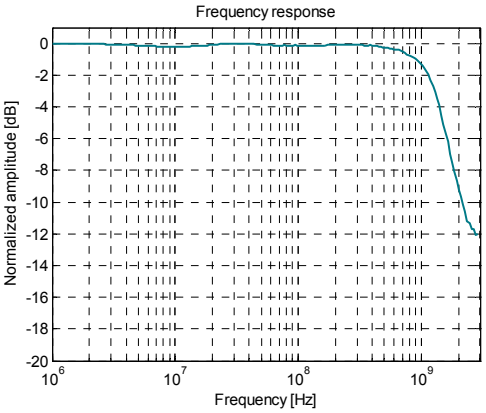
Bandwidth (–3 dB)	1000 MHz
1 dB flatness	800 MHz

Figure 2: ADQ14AC–2X (TBC)



Bandwidth (–3 dB)	700 MHz
1 dB flatness	500 MHz

Figure 3: ADQ14DC–4C



Bandwidth (–3 dB)	1200 MHz
1 dB flatness	900 MHz

Figure 4: ADQ14DC–2X

1. All values are preliminary

5 Spectral performance[1]

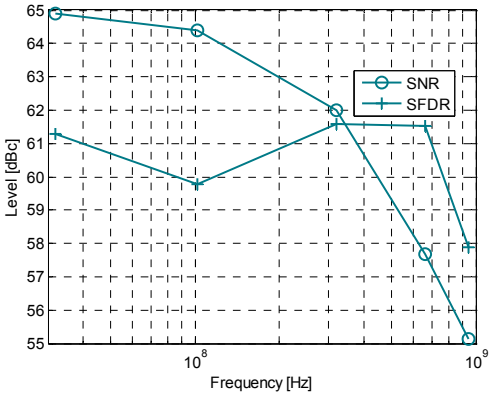


Figure 5: ADQ14AC–4C with overvoltage protection

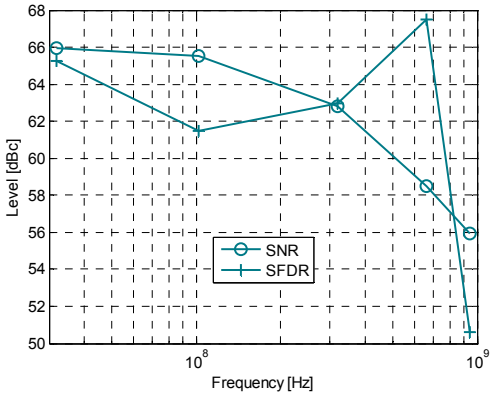


Figure 6: ADQ14AC–2X with overvoltage protection

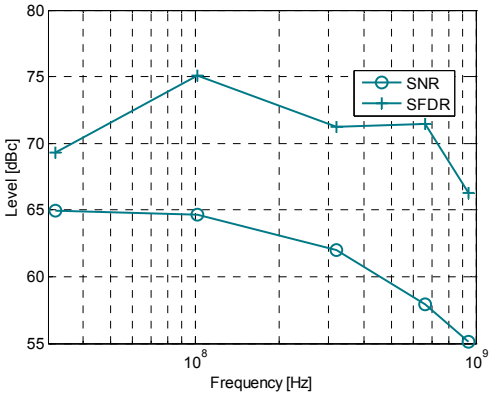


Figure 7: ADQ14AC–4C without overvoltage protection

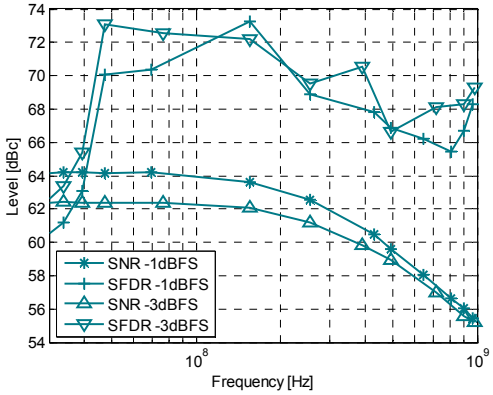


Figure 8: ADQ14AC–2X without overvoltage protection

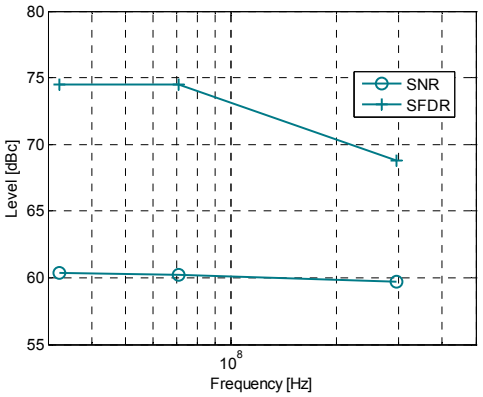


Figure 9: ADQ14DC–4C

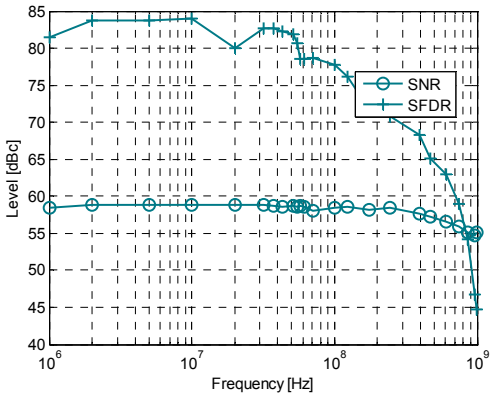


Figure 10: ADQ14DC–2X

1. All values are preliminary

6 Frequency domain[1]

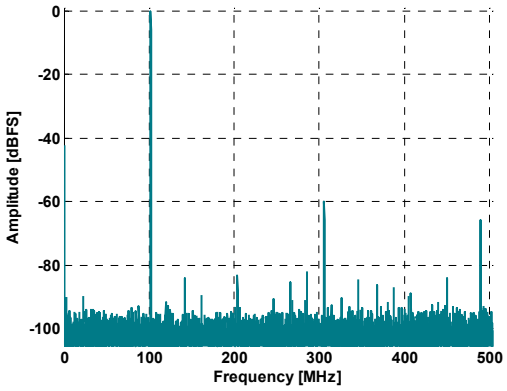


Figure 11: ADQ14AC–4C: 100 MHz with overvoltage protection

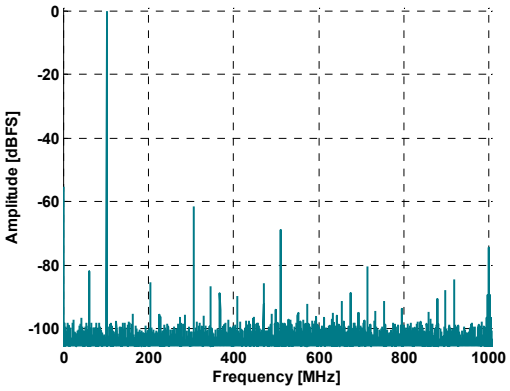


Figure 12: ADQ14AC–2X: 100 MHz with overvoltage protection

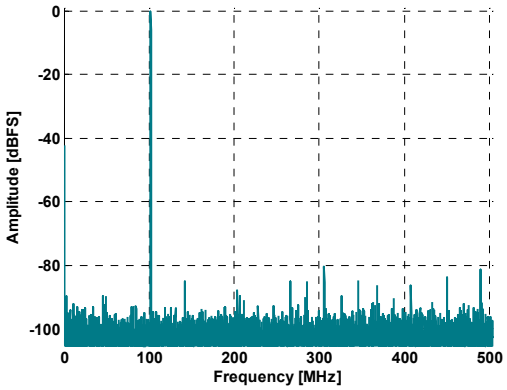


Figure 13: ADQ14AC–4C: 100 MHz without overvoltage protection

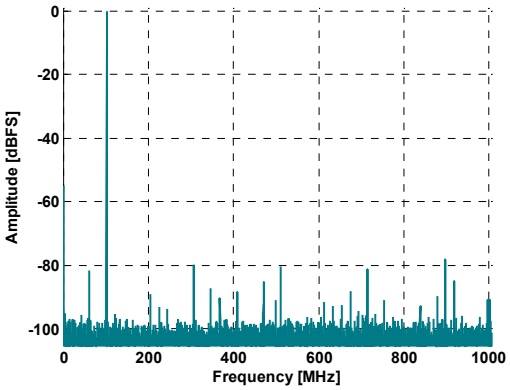


Figure 14: ADQ14AC–2X: 100 MHz without overvoltage protection

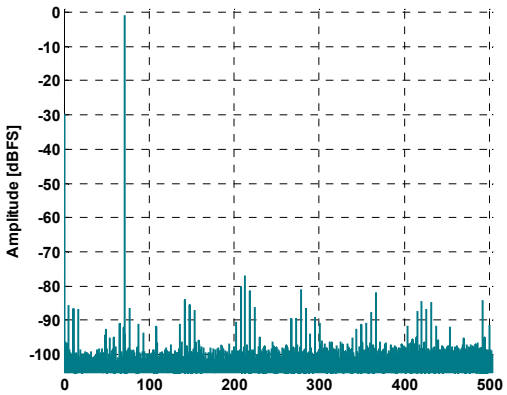


Figure 15: ADQ14DC–4C: 71 MHz

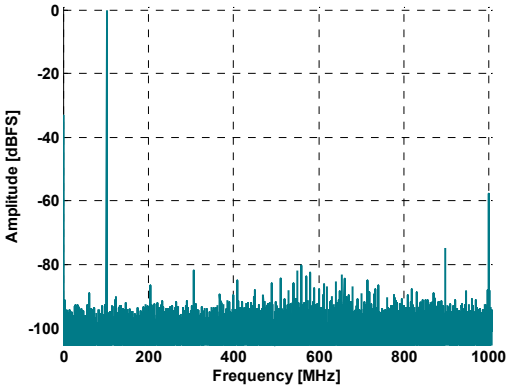


Figure 16: ADQ14DC–2X: 100 MHz

7 Functional overview

7.1 Block diagram

The digitizer includes an analog front-end with signal conditioning, A/D conversion and a digital back-end for data flow control, triggering and host communication, see **Figure 17** and **Figure 18**.

This section describes functions included in the standard data acquisition firmware package –FWDAQ with references to optional functions.

7.2 Data recording

There are several methods for data recording to serve different use cases:

- Continuous multi-record recording using on-board DRAM for very long records.
- Triggered streaming for fast data transfer and long measurement time.
- Continuous streaming of data to the host PC for real-time analysis of data. This mode requires data rate reduction, for example, channel masking, decimation (option –FWSDR), sample skip, or custom implementation using the ADQ14 Development Kit.

To support data recording, there is 2 Gbytes of on-board DRAM. See application note about data acquisition modes for more details.

7.3 Signal processing

There is support for real-time signal processing on the digitizer:

- Level trigger for event detection.
- Gain and offset calibration.
- Real-time waveform averaging (option –FWATD).
- Pulse data zero suppression (option –FWPD).
- DDC and decimation (option –FWSDR).
- Custom real-time signal processing can be implemented in the FPGA using the ADQ14 Development Kit.

7.4 Trigger

There are several trigger modes:

- External for synchronization.
- Level trigger for data driven acquisition.
- Individual level trigger for multi-channel pulse capture (option –FWPD).
- Software for user's control.
- Internal for automatic sequencing.

There is also a trigger output for triggering external equipment. The trigger timing relative the data is controlled by a pre-trigger buffer and the trigger delay parameter. The trigger input and output share the same connector. The trigger output is

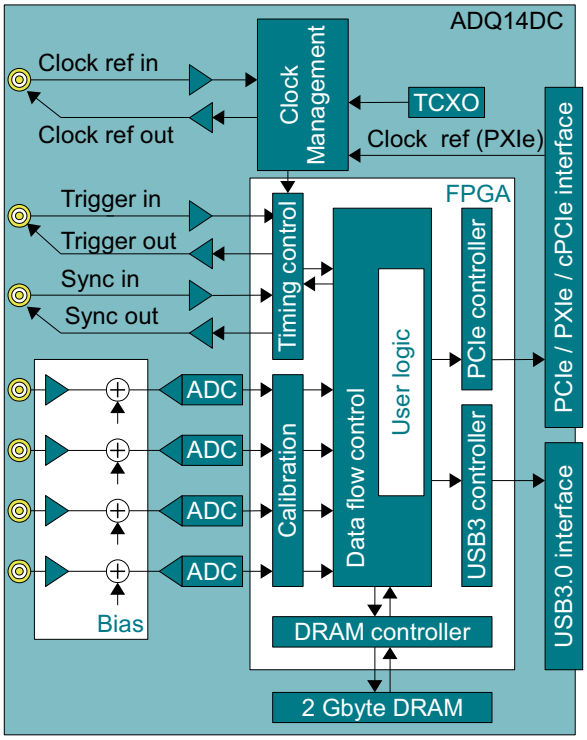


Figure 17: Block diagram 4-channel DC-coupled.

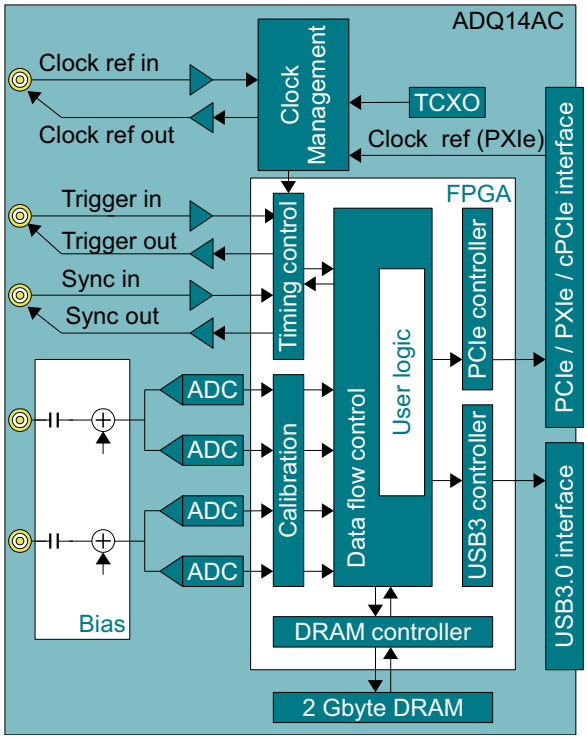


Figure 18: Block diagram 2-channel AC-coupled.

used when the ADQ14 is master and trigger the external equipment. The trigger input is used when the external equipment is master.

7.5 Clock

There are several modes for clocking the digitizer:

- Internal clock for stand alone operation.
- External clock reference input for synchronization where the external equipment acts as master.
- PXIe clock reference from backplane[1].
- Set the sample rate by using sample skip[2].
- External direct clock.

There is also a clock reference output for synchronization where the ADQ14 act as master.

7.6 Multi-unit synchronization

The sync pin is intended for synchronization of a set of digitizers. The synchronization requires firmware option –FWPD.

7.7 GPIO

The GPIO (general purpose digital input output) is intended for communication with external equipment. The GPIO is accessed from the software through register read and write commands. In this way, it is used for creating a link to and from the external equipment to the user's software application.

Real-time interaction with the data flow is also possible through the ADQ14 Development Kit. The GPIO signals are available in the user logic area and can be used for interacting with the data and control in real-time.

The standard version of ADQ14 has GPIO as a software selectable function on the trigger and sync connectors. This means that the connectors are either used as trigger and sync, or as GPIO signals. On the –USB and –PXIE version, the connectors are on the front panel. On the –PCIE version, the trigger is on the front panel whereas the sync is an internal connector on the PCB.

For advanced GPIO requirements, the option –GPIO offers 12 digital signals with individual direction control. The –GPIO option is included in the variable gain option –VG. See **Section 11** for more details.

8 Software tools

8.1 Operating systems

The software package includes drivers for the main operating systems.

8.2 ADCaptureLab

The ADQ14 is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time-domain and frequency-domain analysis, see **Figure 19**. Data can be saved in different file formats for off-line analysis. With ADCaptureLab, the ADQ14 operates as a desktop oscilloscope.

ADCaptureLab is available for Windows only.

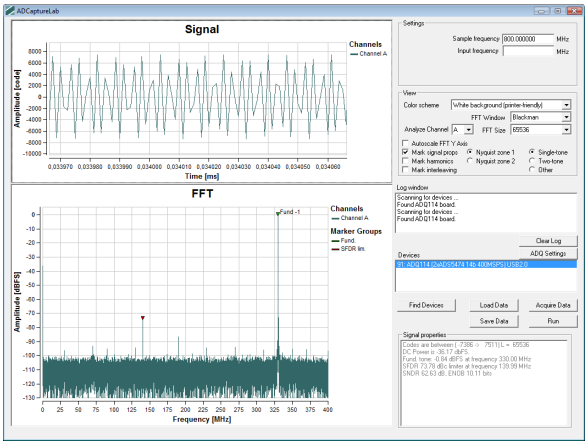


Figure 19: ADCaptureLab (Typical)

8.3 Software development kit (SDK)

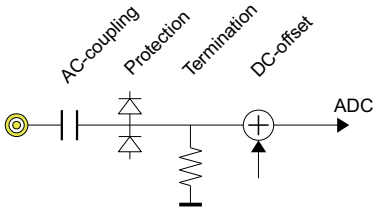
The ADQ14 digitizer is easily integrated into the application by using the software development kit. The SDK is included with the ADQ14.

The SDK includes programming examples and reference projects for several platforms. The ADQAPI reference guide describes all functions in detail. Many examples and application notes simplify the integration process.

Using the SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

1. Option –PXIE and a backplane with clock reference support is required.
2. Sample skip cannot be combined with level trigger nor option –FWPD.

9 Analog front-end options



AC-coupling (ADQ14AC)

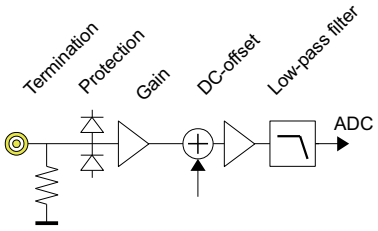
The AC-coupled analog front-end contains overvoltage protection and software programmable DC-offset. The DC-offset is set in 31 steps and the range is covering the full signal range. The settings are user controlled via software.

Then, the overvoltage protection can be turned off for higher linearity at high frequencies. This is done with a software command.

The AC-coupled AFE is preferred where the frequency content is above 300 MHz (approximate limit) where the linearity is better than for the DC-coupled front-end.

The AC-coupled AFE also has the best noise performance.

Note that the AC-coupled AFE is not recommended for signals below 30 MHz.

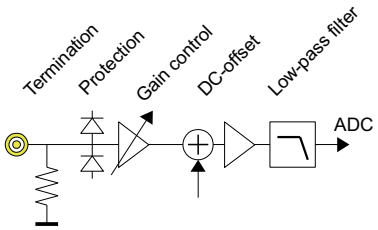


DC-coupling (ADQ14DC)

The DC-coupled analog front-end contains overvoltage protection and software programmable DC-offset. The DC-coupled AFE also has a noise-suppression anti-aliasing filter. The DC-offset is set in 31 steps and the range is covering the full signal range. The settings are user controlled via software.

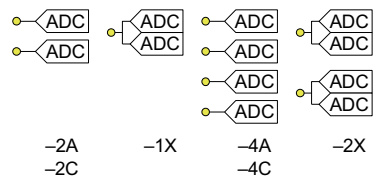
The overvoltage protection is crucial in pulse data systems where high voltage detectors are driving the input. The overvoltage protection reduces the damage at accidental discharges.

The DC-coupled analog front-end is preferred where linearity below 300 MHz (approximate limit) is important.



Variable gain option (ADQ14DC–VG)

The ADQ14DC can be equipped with software-controlled variable gain. Note that the DC-offset is rail-to-rail regardless of the gain setting.

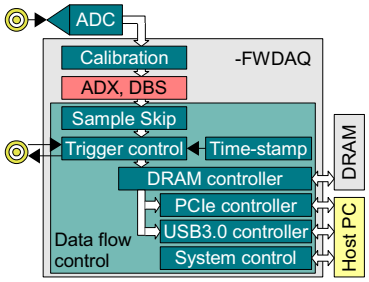


Sample rate and number of channels (–2A, –2C, –1X, –4A, –4C, –2X)

The ADQ14 is available in non-interleaved version (500 MSPS and 1000 MSPS) and in interleaved version (2000 MSPS). The interleaving performance is enhanced by SP Devices' proprietary technology for interleaving, ADX.

ADQ14 is available with 1, 2 or 4 channels depending on the selected sample rate.

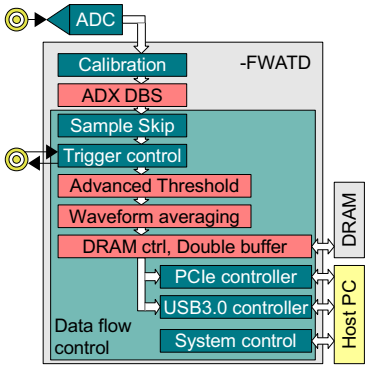
10 Firmware options



Data acquisition firmware (–FWDAQ)

This firmware is always included in the ADQ14. It supports the data acquisition modes continuous multi-record, triggered streaming and continuous streaming. The trigger modes external, internal, software and level trigger are supported as well as internal and external clock reference.

(ADX is included in interleaved models.)



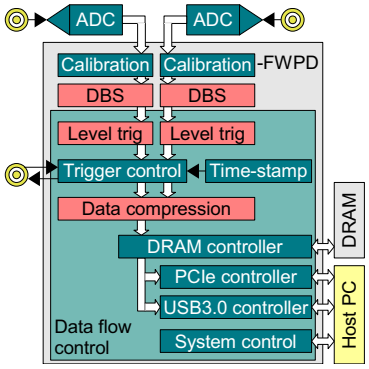
Advanced time-domain (–FWATD)

This firmware option is intended for time-domain analysis of synchronized repetitive events.

It includes advanced threshold algorithm for non-linear discrimination of noise. There is also a waveform averaging (WFA) for real-time accumulation of repetitive events. This contribute to improved SNR. The WFA can take waveforms up to 1 MSamples in length. The WFA may also be split into several accumulations of a total length up to 1 MSamples to simplify read-out scheduling.

The DBS algorithm is used for achieving a stable baseline.

(Available Q1 2016)

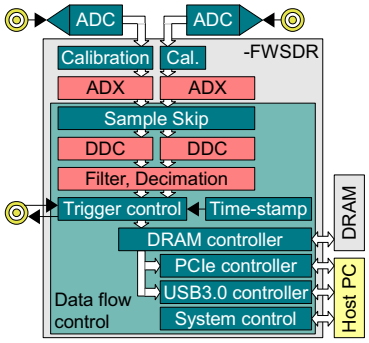


Pulse data (–FWPD)

This firmware is optimized for capturing random events. Each channel is individually event-triggered. Trigger level is a user-defined level or a filtered data for adaptive thresholding. The record length is dynamic for random event length. Data compression through zero suppression saves disk space.

The DRAM of 2 GByte is used as a data FIFO to buffer bursts of events before transferring data to the host PC.

The DBS algorithm is used for achieving a stable baseline.

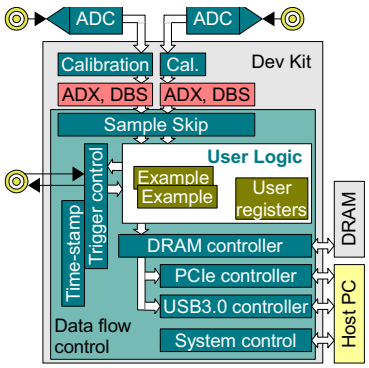


Software defined radio (–FWSDR)

This firmware implements software defined radio functions. It includes digital down conversion and decimation. After decimation the data rate is well adapted to streaming to the host PC.

(Availability TBD.)

11 Feature enhancement options

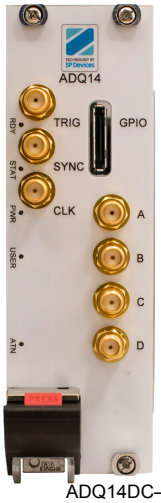


Getting real-time custom signal processing firmware through the ADQ14 Development Kit

The ADQ14 is equipped with an powerful Xilinx Kintex 7 K325T FPGA which is partly available for customized real-time applications.

SP Devices' ADQ14 Development Kit is an optional FPGA design project that enables custom real-time signal processing of streaming data. More details about this product can be found in the datasheet for the ADQ Development Kit.

The ADQ14 Development Kit is purchased separately.



ADQ14DC–4C–VG–PXIE

GPIO for connecting to external equipment (–GPIO)

The option for general purpose digital input and output (–GPIO) offers digital bi-directional signals. The direction of each pin is set individually. The signal level is 3.3V CMOS or LVDS.

The signals are accessed from the API through read and write commands to the corresponding registers. The direction is also set from software. At start-up, all pins are default inputs. The GPIO can also be accessed in the FPGA via the ADQ14 Development Kit for real-time interaction with the data flow.

The variable gain option, –VG, always includes the –GPIO option.

Additional to the –GPIO option, a custom GPIO expansion card can be provided. The design of a custom GPIO expansion card is available through SP Devices' design service. Please contact an SP Devices' sales representative for more information.

12 Data interface options

ADQ14-4C-USB

Stand-alone operation with USB3.0 interface (–USB)

The SuperSpeed USB3.0 interface is intended for stand-alone operation and allows the ADQ14 to be physically integrated with the detector rather than the host PC. This means that the cable between the detector and the digitizer is kept as short as possible for optimized signal quality. The USB box includes flanges for fastening of the box and screw attachment of the USB cable.

With the USB3.0 interface, the digitizer is easily connected to any computer. The sustained data rate can be up to 200 MBytes/s and combined with on-board signal processing, an efficient solution is available.

ADQ14DC–4C–VG–PXIE

Modular instrumentation with cPCIe / PXIe (–PXIE)

The cPCIe / PXIe form factor is intended for integration into a chassis for modular instrumentation or large scale acquisition. The ADQ14 can operate in Compact PCI Express or PXI Express chassis. Using the multi-unit sync function, multi-channels systems can be achieved.

Use peer-to-peer streaming at up to 3.2 GBytes/s for sending data to disk or additional computational FPGA cards (ADQDSP).

In a PXI Express chassis, the clock reference from the backplane can be used as clock reference for the digitizer.

ADQ14DC–2X

Systems integration with PCIe interface (–PCIE)

The PCIe form factor is for integration into the host PC. The high speed PCIe interface can handle data rates up to 3.2 GBytes/s. This is specially useful when combining the digitizer with heavy computation in, for example, a GPU in the same PC. The board is half length to enable compact solutions.

ADQ14DC–4C–MTCA

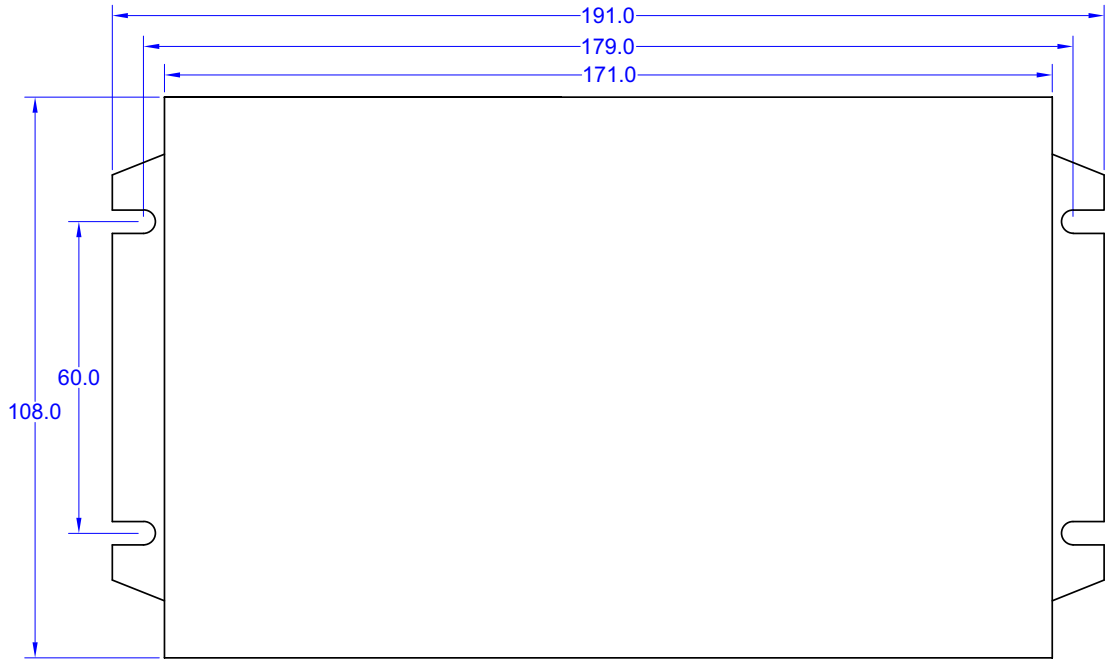
Large scale integration with Micro-TCA.4 (–MTCA)

The Micro-TCA.4 form factor is intended for integration into a chassis for modular instrumentation or large scale data acquisition.

The Micro-TCA.4 card is equipped with the –GPIO option as standard. (The variable gain option, –VG, is not available.)

13 Appendix

13.1 USB fastening



13.2 Cable attachment

All cables have lock function so that no cable should fall out unintentionally.

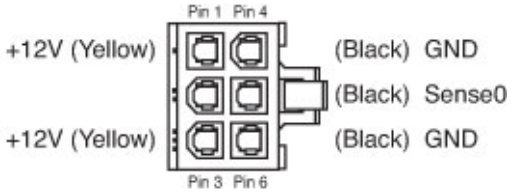
FUNCTION	CONNECTOR	–USB	–PCIE	–PXIE	–MTCA	LOCK FUNCTION
Analog	SMA	✓	✓	✓	✓	Screw
Trigger	SMA	✓	✓	✓	✓	Screw
Clock ref	SMA	✓	✓	✓	✓	Screw
Sync	SMA	✓		✓	✓	Screw
Sync	MCX		✓			Snap lock. Placed internally in PC chassis
Power	DIN	✓				Snap lock
Power	Backplane			✓	✓	Screw attached board in chassis
Power	PCIe Aux		✓			Snap lock
GPIO	Hirose	✓	✓	✓	✓	Snap lock
Data/control	USB3.0	✓				Screw attachment vision USB standard[1]
Data/control	Backplane		✓	✓	✓	Screw attached board in chassis

1. Optional cable solution. Not included in standard shipment.

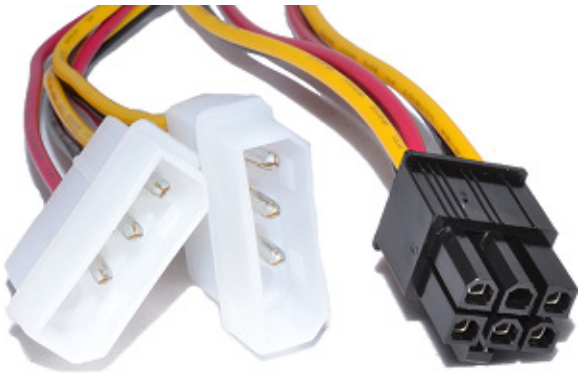
13.3 Power supply of –PCIE card

The ADQ14–PCIE is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary 75W power supply connector. The connection in the cable should be as in **Figure 20** (a). Some power supplies do not have this connector and an adapter as in **Figure 20** (a) is required.

It is important that the axillary power supply is turned on immediately when the PC start. Otherwise, the digitizer will not be recognized on the PCI Express bus.



(a) Cable connection



(b) Cable adapter example

Figure 20: Power supply of –PCIE

13.4 Micro-TCA backplane connectors

PORT	FUNCTION	SIGNALING	ADQ14–MTCA AVAILABILITY
0, 1	1 GbE	N/A	N/A
2, 3	SAS/SATA	N/A	N/A
4, 5, 6, 7	PCIe	PCIe Gen2 x4	Main data and control interface
8, 9, 10, 11	SRIO	N/A	N/A
12, 13, 14, 15	P-t-P	High speed serial	Available through ADQ14 Development Kit only
16	TCLKC/D	N/A	N/A
17, 18, 19, 20	Tr/clk/int	LVDS	Available through ADQ14 Development Kit only
Clk 1	TCLKA	LVPECL	Clock reference, select from API
Clk 2	TCLKB	LVPECL	Clock reference, select from API
Clk 3	FCLKA	PCIe clock	PCIe interface reference clock

Available through the ADQ14 Development Kit only means that the physical connection is on the board, but there is no function defined for the signal. The signals are available for inclusion in custom firmware in the FPGA. The custom firmware is designed using the ADQ14 Development Kit.

13.5 LED definitions

COLOR	NAME	FUNCTION	STATE
Green	Power	Power on	On: Power on and FPGA is operating
Yellow	Ready	Waiting for trigger	The ADQ14 is set up to accept trigger and wait for the trigger
Red	Status	Overheat	Flashing means overheating or fan fault.
Blue	User	Custom	On during initialization of the board. Available for custom implementation in ADQ14 Development Kit
Red	Attention	Attention LED for PXIe	Attention LED for PXIe

Ordering information

ORDERING INFORMATION	
ADQ14 AC-coupled	ADQ14AC
ADQ14 DC-coupled	ADQ14DC
AVAILABLE OPTIONS	
Host PC interface	–USB, –PCIE, –PXIE, –MTCA
Analog front-end options	–2A, –2C, –1X, –4A,–4C, –2X, –VG
Firmware options	–FWDAQ, –FWATD[1], –FWPD, –FWSDR[2]
GPIO option	–GPIO
RELATED PRODUCTS	
ADQ14 Development Kit	ADQ14 Development Kit
ADQ14–GPIO cable assembly 1m 2 connectors	108-004-003
USB3.0 cable with screw lock	108-002-006

1. Beta release available 2015 Q4
2. Availability TBD

References

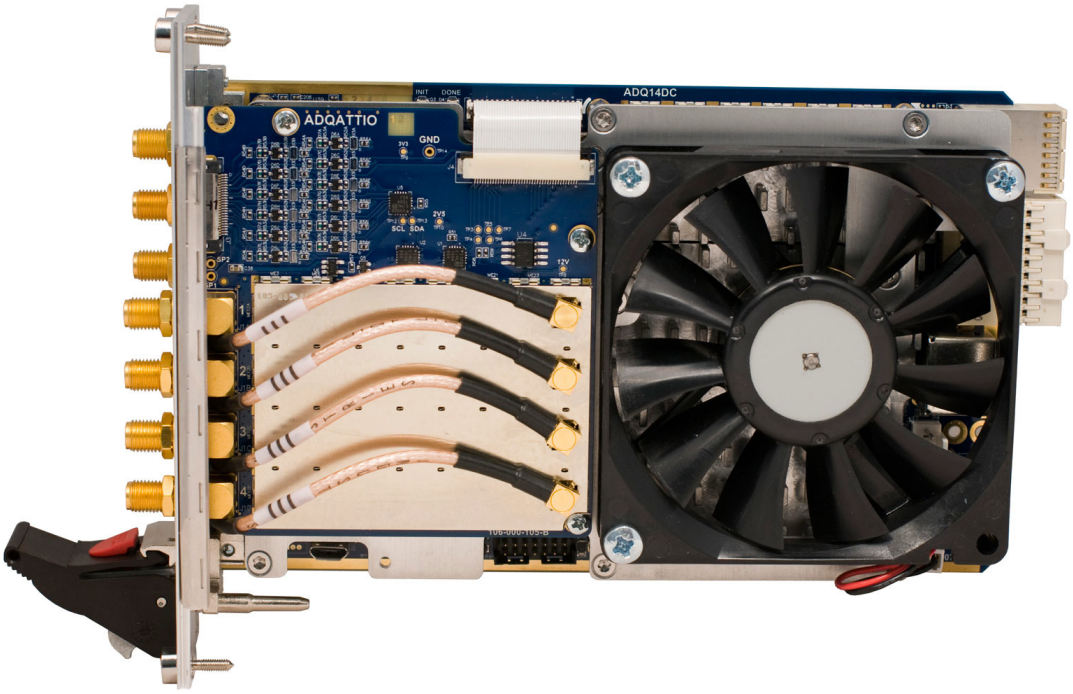
14-1397 ADQ14-FWATD datasheet

15-1455 ADQ14-FWPD datasheet

15-1469 ADQ14-FWSDR datasheet

15-1468 ADQ14 LabVIEW app note

15-1413 ADQ14-GPIO datasheet



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