



3U VPX, Virtex 7 FPGA Triple QSFP+ interfaces Conduction or Air-Cooled





High Speed Data Conversion

& Signal Processing Solutions

AV 109

Applications

- Real time processing
- Wideband data communication
 Data storage interface

- Features
- Three QSFP (Quad Small Form-Factor Pluggable) interface
- Supports QSFP copper or optical
- transceivers up to 10 Gbps/lane
- Three on board low jitter reference clock generators
- User programmable Xilinx® Virtex® 7 VX415T or VX690T FPGA
- Two banks 667 MHz 256M16 DDR3 SDRAM
- · 3U OpenVPX standard compliant
- Air cooled and Conduction cooled rugged versions
- rugged versions
 FPGA firmware cores
- FPGA TIrmware cores
- \cdot Windows® and Linux® drivers

Quad Small Form-Factor Pluggable Transceiver

The AV109 supports three independent Quad Small Form-Factor Pluggable (QSFP) transceivers.

The AV109 supports optical QSFP transceivers for communication at up to 120 Gbps over distances up to 10 km.

The AV109 supports copper QSFP transceivers for communication at up to 120 Gbps over distances up to a few meters.

Clocks

The AV109 provides three on-board, user programmable, low jitter clock generator generating clock references as required for the high speed serial links (Xilinx Virtex® 7 GTH). The clock frequency can be selected among the following:

- 100 MHz, supporting PCIe gen 1
- 106.25 MHz, supporting Serial FPDP and Fibre Channel
- 125 MHz, supporting PCIe gen 1, GigE, Aurora and SRIO 1.25 and 2.5 Gbps
- 150 MHz, supporting SATA
- 156.25 MHz, supporting XAUI, SRIO and Aurora 3.125 Gbps
- 159.375 MHz, supporting 10-G Fibre Channel
- 250 MHz, supporting PCIe gen 2
- 312.5 MHz, supporting Aurora 5 and 6.25 Gbps

FPGA

The AV109 is fitted with a Xilinx Virtex 7 VX415T or VX690T user programmable FPGA. Only few resources are used to control and communicate with external hardware such as DDR3 SDRAM and monitoring subsystem, leaving most of the logic and block

Overview

The AV109 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the ANSI/VITA 65, OpenVPX standard.

The AV109 is fully compliant with the OpenVPX standard, with default support for the MOD3-PAY-2F1F2U-16.2.1-3 and MOD3-PAY-2F1F2U-16.2.1-4 module profiles, PCIe Gen 1 or Gen 2 on Data Planes and Expansion Plane plus 1000BASE-BX on Control planes.

The AV109 combines the very high processing power delivered by Xilinx® Virtex® 7 FPGA with three independent QSFP (Quad Small Form-Factor Pluggable) interface, making it ideally suited for embedded signal processing applications for data communication and data storage interface with support for datarate at up to 10 Gbps per link.

The AV109 provides three on board, user programmable, low jitter clock generator supporting reference clocks as required for PCle, SATA, SRIO, Fiber Channel, Aurora, Gbit Ethernet or XAUI protocols.

The AV109 includes one Xilinx® Virtex® 7 FPGA VX415T or VX690T for an impressive processing capability of up to more than 2 TMACs (Multiply Accumulate per second), two banks 667 MHz 256M16 DDR3 SDRAM memory for data processing and a 1 Gb synchronous FLASH memory for multiple firmware storage.

The AV109 features a 32-bit microcontroller with USB 2.0 and 10/100 Ethernet interfaces intended to be used for system monitoring and supervision.

The AV109 comes with complete software drivers for Windows and Linux. An FPGA firmware package is provided including all cores necessary to build user FPGA applications.

RAM and all DSP resources available for customer processing.

Dedicated to signal processing, the Xilinx Virtex 7 VX415T FPGA includes 412,160 logics cells, 880 bloc RAM (36 Kbit each), 2,160 DSP48E1 slices and 2 PCIe interface blocs. The most powerful version embeds a Xilinx Virtex 7 VX690T which provides 693,120 logics cells, 1,470 bloc RAM and 3,600 DSP48E1 slices for an impressive processing power of more than 2 TMACs.

The FPGA is delivered in -2 speed grade.

FLASH Memory

The AV109 includes two 667 MHz 256M16 DDR3 SDRAM memory banks and one 1 Gbit synchronous BPI FLASH used to store multiple FPGA configuration files.

VPX interface

The AV109 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1. The AV109 also supports a USB2.0, a 10/100 Ethernet and 24 LVDS differential pairs on P2.

The AV109 features two low phase noise clock generators able to synthesize clock references for the FPGA GTXs from 100 MHz to 312.5 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1 and Gen 2, SATA, SRIO and XAUI 10Gbit Ethernet up to 12.5 Gbps.

Microcontroller

The AV109 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision. The microcontroller supports USB 2.0 and 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/ VITA 46.10 compliant custom RTM board.

The microcontroller firmware includes all necessary features for board monitoring and supervision, including FPGA firmware downloads through Ethernet or USB.

Firmware

The AV109 comes with a firmware package which includes VHDL cores allowing control and communication with all AV109 hardware resources.

A base design is provided which demonstrates the use of the AV109 and gives users a starting point for firmware development. The AV109 firmware package is supported on the Xilinx VIVADO® 2012.4 design suite and later.

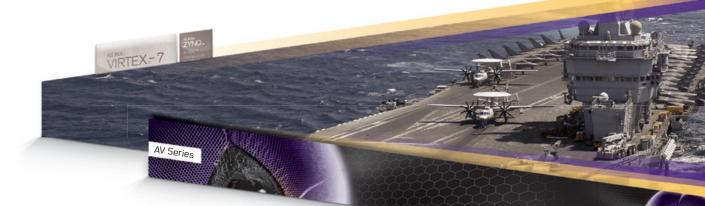
Software

The AV109 is delivered with control software for Windows 7 and Linux.

Ruggedization

The AV109 is delivered in air-cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.

Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.



Specifications

QSFP cage and connector

- · Compliant with QSFP standard
- · 38-contact QSFP connector

Reference Clock

- · 100 MHz, supported protocols: · PCle gen 1
- · 106.25 MHz, supported protocols:
- · Serial FPDP, 1 and 2 Gbps
- Fibre Channel 1 and 2 Gbps
- · 125 MHz, supported protocols: · PCle gen 1
- GigE
- · Aurora 1.25 and 2.5 Gbps
- · 150 MHz, supported protocols: · SATA 1.5 and 3 Gbps
- 156.25 MHz, supported protocols:
- · XAUI 3.125 Gbps
- SRIO 3.125 Gbps
- · Aurora 3.125 Gbps
- · 250 MHz, supported protocols:
- · PCle gen 2
- · 312.25 MHz, supported protocols: Aurora 5 and 6.25 Gbps

FPGA

- FPGA: Xilinx Virtex 7
- · XC7VX415T-2FFG1158 or
- · XC7VX690T-2FFG1158 Memory · 1 bank 256M32 DDR3 SDRAM,
- 667 MHz clock
- One 1 Gbit NOR FLASH memory

VPX interface

- P1:
 - · Data plane: two fat pipes
 - Expansion plane: one fat pipe
 - · Control plane: 2 ultra-thin pipes
 - · 2 user-defined ultra-thin pipes
- P2:
- · USB2.0 and 10/100 Ethernet
- · 24 LVDS differential pairs

Software support

OSEP

QSFP

QSEP

25 MHz

- · Software Drivers: • Windows 7
- Linux

Fiber of

Fiber o

Fiber o

- · Application example:
- · Windows and Linux

Firmware support

· VHDL cores for all hardware

resources

- · Base design
- Supported by Xilinx VIVADO 2012.4 and later
- Ruggedization
- · As per VITA 47:
- · Air cooled : EAC4 and EAC6
- · Conduction cooled : ECC3 and ECC4

Power dissipation

Power Supp DC/DC

Monitoring

1 Gb BPI Flash

DP01

DP02

- Fat Pipe x1

2x Ultra-thin Pipe

2x Ultra-thin Pig

LVDS pairs x2

12C

10/100 Eth

USB

- · +12V: 6.9 A max (83W)
- · +5V: 8.8 A max (44W)
- · +3.3V: 0.5 A max (1.6W)
- · +3.3VAUX: 0.3 A max (1.1W)

Weight

AV109

VIRTEX 7 FPGA

VX415T

VX690T

-2FFG11581

GTH x4

I2C - CTRL

GTH x4

I2C - CTRL

GTH x4

I2C - CTRL

Clock

2 x 256M16 533 MHz DDR3 SDRAM

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- · Air cooled : 550g
- · Conduction cooled : 650g

Ordering information

Part Number		Α	۷	109	- 1	гг	-	а
Ruggedization level	Air Standard			-				-
	Air Rugged	-	-	-	-	AR	-	-
	Conduction Standard	-	-	-	-	CS	-	-
	Conduction Rugged	-	-	-	-	CR	-	-
Options 1	FPGA Virtex 7 VX415T-2	-	-	-	-	-	-	1
	FPGA Virtex 7 VX690T-2	-	-	-	-	-	-	2



- APISSYS
- OpenVPX

P0

P1

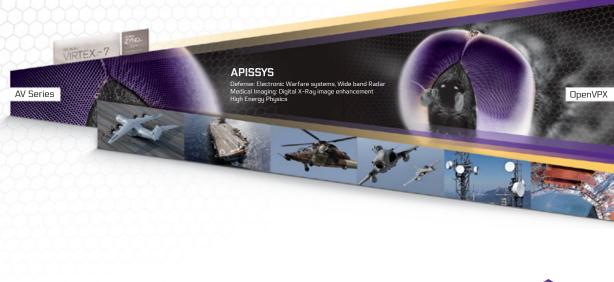
P2

High Speed Data Conversion & Signal Processing Solutions

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (1) (8 CFM airflow at sea level)	-40 to +70°C (1) (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (default acrylic 1B31)	Yes (default acrylic 1B31)	Yes (default acrylic 1B31)

www.apissys.com





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