AV104

Radar Emitter-Receiver DRFM

3U VPX, Virtex 7 FPGA
Dual 10 bit 3 Gsps ADC
Single 12 bit 3 Gsps DAC
Conduction or Air-Cooled

ApisSys

High Speed Data Conversion
& Signal Processing Solutions

AV104

Applications

- Real time processing
- Electronic Warfare - DRFM
- Wideband Radar
- LIDAR

Features

- 2 channels 10-bit, 3 Gsps ADC
- 1 channel 12-bit, 3 Gsps DAC
- External clock and reference input
- Low jitter Internal clock generation
- External trigger input
- User programmable Xilinx® Virtex® 7VX330T to VX690T FPGA
- 500 MHz 2M x 36 QDRII+ SRAM
- 3U OpenVPX standard compliant
- Air cooled and Conduction cooled rugged versions
- FPGA firmware cores
- Windows® and Linux® drivers

Overview

The AV104 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the ANSI/VITA 65, OpenVPX standard.
The AV104 is fully compliant with the OpenVPX standard, with default support for the MOD3-PAY-2F1F2U-16.2.1-3 and MOD3-PAY-2F1F2U-16.2.1-4 module profiles, PCIe Gen 1 or Gen 2 on Data Planes and Expansion Plane plus 1000BASE-BX on Control planes.
The AV104 combines the very high processing power delivered by Xilinx® Virtex® 7 FPGA with two channels 10-bit 3 Gsps ADCs and one channel 12-bit 3 Gsps DAC, making it ideally suited for embedded signal processing applications such as Electronic Warfare, Wideband Radar Transmitter/Receivers or LIDAR.
The AV104 provides an internal ultra low jitter clock generation and can be used with either an external clock or an external reference for higher flexibility.
The AV104 includes one Xilinx® Virtex® 7 FPGA VX330T/VX485T or VX690T for an impressive processing capability of up to more than 2 TMACs (Multiply Accumulate per second), one high speed 2M36 QDRII+ SRAM memory for data processing and a 1 Gb synchronous FLASH memory for multiple firmware storage.
The AV104 features a 32-bit microcontroller with USB 2.0 and 10/100 Ethernet interfaces intended to be used for system monitoring and supervision.
The AV104 comes with complete software drivers for Windows and Linux. An FPGA firmware package is provided including all cores necessary to build user FPGA applications.

10-bit 3 GSPS ADC

The AV104 Analog to Digital conversion is performed by two 10-bit 3 Gsps ADCs.
The AV104 provides two front panel SSMC connectors for analog input.
Single ended input signals are AC coupled with an input bandwidth of 5 MHz to 3 GHz or 700 MHz to 4 GHz with 2 dBm input level.

12-bit 3 GSPS DAC

The AV104 Digital to Analog conversion is performed by one 12-bit 3 Gsps ADCs.
The AV104 provides one front panel SSMC connector for analog output. Single ended output signal is AC coupled with an output bandwidth of 5 MHz to 3 GHz or 700 MHz to 4 GHz with -2 dBm output level.

Clock

The AV104 provides an internal ultra low jitter clock generator locked on a 100 MHz internal reference.
The AV104 provides a front panel SSMC connector for a 10 to 100 MHz external reference, a front panel SSMC connector for a 500 MHz to 3 GHz external clock input, and a front panel SSMC connector for an external clock output.
Estimated jitter from the internal clock generation (100 MHz reference and clock distribution) is below 200 fs for a 3 GHz clock. Added jitter on external clock is lower than 100 fs.

Trigger and Synchronization

The AV104 provides a front panel SSMC connector for external trigger input. The trigger synchronization uses the sampling clock divided by 8.

FPGA

The AV104 is fitted with a Xilinx Virtex 7 VX330T/VX485T or VX690T user programmable FPGA. Only few resources are used to control and communicate with external hardware such as QDRII+ SRAM and monitoring sub-system, leaving most of the logic and block RAM and all DSP resources available for customer processing.
Dedicated to signal processing, the Xilinx Virtex 7 VX485T FPGA includes 485,760 logics cells, 1,030 bloc RAM (36 Kbit each), 2800 DSP48E1 slices and 2 PCIe interface blocs.
The most powerful version embeds a Xilinx Virtex 7 VX690T which provides 693,120 logics cells, 1,470 bloc RAM and 3,600 DSP48E1 slices for an impressive processing power of more than 2 TMACs.
The FPGA is delivered in -2 speed grade.

QDRII+ SRAM Memory

The AV104 includes one 2M36 QDRII+ SRAM memory clocked at 500 MHz for a peak data rate of 9 GB/s.

FLASH Memory

The AV104 includes one 1 Gbit synchronous BPI FLASH used to store multiple FPGA configuration files.

VPX interface

The AV104 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1. The AV104 also supports a USB2.0, a 10/100 Ethernet and 24 LVDS differential pairs on P2.
The AV104 features two low phase noise clock generators able to synthesize clock references for the FPGA GTXs from 100 MHz to 312.5 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1 and Gen 2, SATA, SRIO and XAUI 10Gbit Ethernet up to 12.5 Gbps.

Microcontroller

The AV104 features a 32-bit 80 MHz microcontroller used primarily for board monitoring and supervision.
The microcontroller supports USB 2.0 and 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board.
The microcontroller firmware includes all necessary features for board monitoring and supervision, including FPGA firmware downloads through Ethernet or USB.

Firmware

The AV104 comes with a firmware package which includes VHDL cores allowing control and communication with all AV104 hardware resources.
A base design is provided which demonstrates the use of the AV104 and gives users a starting point for firmware development. The AV104 firmware package is supported on the Xilinx ISE® 14 design suite and later.

Software

The AV104 is delivered with control software for Windows 7, and Linux.
Ruggedization
The AV104 is delivered in air-cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.
Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.

Specifications

Analog Input/Output

- Coupling: AC
  - Full power bandwidth up to 4GHz
  - Full scale : 2 dBm
- Connector: SSMC, 50 Ohm

Analog – Digital Conversion

- Two channels
- Resolution: 10 bit
- Sampling Frequency up to 3 GHz
- 3 Gsps, Fin = 2.6 GHz, -1dBFS:
  - SNR: 49 dBFS
  - SFDR: 52 dBc
  - ENOB: 7.6 bits

Digital – Analog Conversion

- One channel
- Resolution: 12 bit
- Sampling Frequency up to 3 GHz
- 3 Gsps, Fout = 2.6 GHz, -1dBFS:
  - Noise density: < -150 dBm/Hz
  - SFDR 2nd Nyquist: 50 dBc

Clock

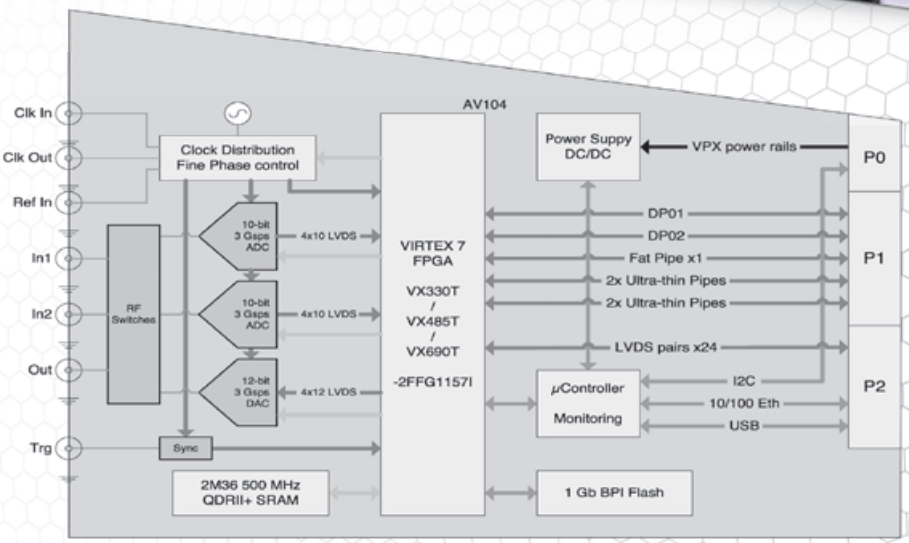
- Internal: 500 MHz to 3 GHz low jitter clock, Internal jitter: < 200 fs
- External Input Clock:
  - frequency: 500 MHz to 3 GHz
  - Connector: SSMC, 50 Ohm
- External Output Clock:
  - frequency: sampling clock
  - Connector: SSMC, 50 Ohm
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Connector: SSMC, 50 Ohm

Trigger

- External: 0 to 2Vp,
  - Connector: SSMC

FPGA

- FPGA: Xilinx Virtex 7
  - XC7VX330T-2FFG1157 or
  - XC7VX485T-2FFG1157 or
  - XC7VX690T-2FFG1157



Memory

- 1 bank 2M x 36-bit QDRII+ SRAM, 500 MHz clock
- One 1 Gbit NOR FLASH memory

VPX interface

- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 24 LVDS differential pairs

Software support

- Software Drivers:
  - Windows 7
  - Linux
- Application example:
  - Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx ISE 13 and later

Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3 and ECC4

Power

- +12V: 5 A max (60W)
- +5V: 7.4 A max (37W)
- +3.3V: 0.5 A max (1.6W)
- +3.3VAUX: 0.3 A max (1W)

Weight

- Air cooled : 500g
- Conduction cooled : 500g

Ordering information

Part Number		A	V	104	-	rr	-	a	b
Ruggedization level	Air Standard	-	-	-	-	AS	-	-	-
	Air Rugged	-	-	-	-	AR	-	-	-
	Conduction Standard	-	-	-	-	CS	-	-	-
	Conduction Rugged	-	-	-	-	CR	-	-	-
Options 1	FPGA Virtex 7 VX330T-2	-	-	-	-	-	-	1	-
	FPGA Virtex 7 VX485T-2	-	-	-	-	-	-	2	-
	FPGA Virtex 7 VX690T-2	-	-	-	-	-	-	3	-
Options 2	Input/Output bandwidth 5 MHz to 3000 MHz	-	-	-	-	-	-	-	1
	Input/Output bandwidth 700 MHz to 4000 MHz	-	-	-	-	-	-	-	2

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (1) (8 CFM airflow at sea level)	-40 to +70°C (1) (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (default acrylic 1B31)	Yes (default acrylic 1B31)	Yes (default acrylic 1B31)

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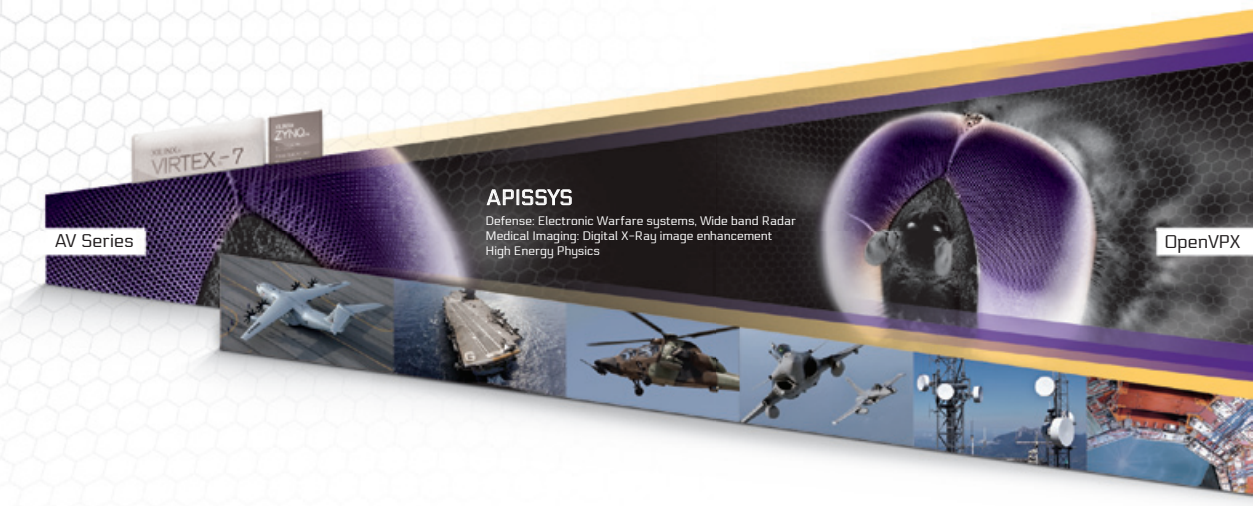
Design By vert-pomme.ch - 04.2013



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