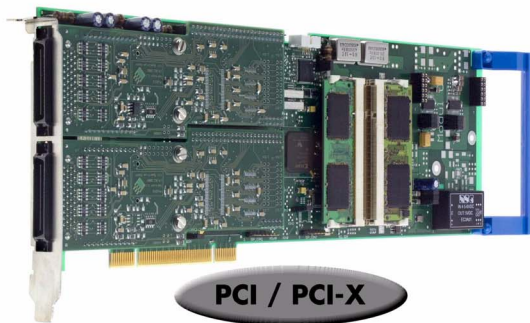


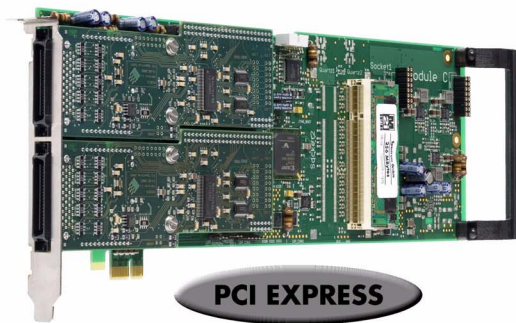


M2i.70xx - 64 bit fast digital waveform acquisition/pattern generator

- 16, 32 or 64 bit digital I/O
- 1 kS/s up to 125 MS/s at 16 and 32 bit
- 1 kS/s up to 62.5 MS/s at 32 and 64 bit
- 110 Ohm input impedance selectable
- Inputs 3.3 V and 5 V TTL compatible
- Up to 2 GByte on-board memory
- 512 MByte standard memory installed
- FIFO mode for input and output
- Pattern/edge/pulse width/delay trigger
- Synchronization of up to 16 cards per system and up to 271 cards with system sync
- Features: Multiple Recording/Replay, Gated Sampling/Replay, BaseXIO



PCI / PCI-X



PCI EXPRESS

- 66 MHz 32 bit PCI-X interface
- 5V / 3.3V PCI compatible
- 100% compatible to conventional PCI > V2.1
- Sustained streaming mode up to 245 MB/s

- 2,5 GBit x1 PCIe Interface
- Works with x1/x4/x8/x16* PCIe slots
- Software compatible to PCI
- Sustained streaming mode up to 160 MB/s

<u>Operating Systems</u>	<u>Recommended Software</u>	<u>Drivers and Examples</u>
<ul style="list-style-type: none"> • Windows XP, Vista, 7, 8, 10 • Linux Kernel 2.4, 2.6, 3.x, 4.x • Windows/Linux 32 and 64 bit 	<ul style="list-style-type: none"> • SBench 6 • MATLAB • LabVIEW, LabWindows/CVI 	<ul style="list-style-type: none"> • Visual Basic, C/C++, GNU C+ • Borland Delphi, .VB.NET, C#, J# • Python

Model	1-4 bit	8 bit	16 bit	32 bit	64 bit
M2i.7005	125 MS/s	125 MS/s	125 MS/s		
M2i.7010		125 MS/s	125 MS/s		
M2i.7011		125 MS/s	125 MS/s	62.5 MS/s	
M2i.7020		125 MS/s	125 MS/s	125 MS/s	
M2i.7021		125 MS/s	125 MS/s	125 MS/s	62.5 MS/s

General Information

The M2i.70xx series of fast digital I/O boards offer a resolution between 1 bit and 64 bit with a maximum sampling rate of 125 MS/s (62.5 MS/s). All I/O lines of the card can be programmed for either input or output direction. The on-board memory of up to 2 GByte can be used completely for recording or replaying digital data. Alternatively the M2i.70xx can be used in FIFO mode. All boards of the M2i.70xx series may use the whole installed on-board memory completely for the currently activated number of channels. Then data is transferred on-line to PC memory or hard disk. The internal standard synchronisation bus allows synchronisation of several M2i series cards. Therefore the M2i.70xx board can be used as an enlargement to analog boards.

*Some x16 PCIe slots are for the use of graphic cards only and can not be used for other cards.

Software Support

Windows drivers

The cards are delivered with drivers for Windows XP, as well as Vista, Windows 7 and Windows 8 (each 32 bit and 64 bit). Programming examples for Visual C++, Borland C++ Builder, LabWindows/CVI, Borland Delphi, Visual Basic, VB.NET, C#, J# and Python are included.

Linux Drivers



All cards are delivered with full Linux support. Pre-compiled kernel modules are included for the most common distributions like RedHat, Fedora, Suse, Ubuntu LTS or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++ as well as the possibility to get the driver sources for your own compilation.

SBench

A full licence of SBench the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. The version 6 is running under Windows as well as under Linux (KDE and GNOME).

Third-party products

Spectrum supports the most popular third-party software products such as LabVIEW, MATLAB or LabWindows/CVI. All drivers come with detailed documentation and working examples are included in the delivery. Support for other software packages, like VEE or DasyLab, can also be provided on request.

Hardware features and options

PCI/PCI-X



The cards with PCI/PCI-X bus connector use 32 Bit and up to 66 MHz clock rate for data transfer. They are 100% compatible to Conventional PCI > V2.1. The universal interface allows the use in PCI slots with 5 V I/O and 3.3 V I/O voltages as well as in PCI-

X or PCI 64 slots. The maximum sustained data transfer rate is 245 MByte/s per bus segment.

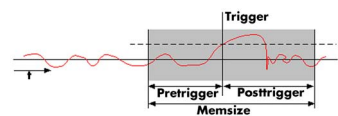
PCI Express



The cards with PCI Express use a x1 PCIe connector. They can be used in PCI Express x1/x4/x8/x16 slots, except special graphic card slots, and are 100% software compatible to Conventional PCI > V2.1. The maximum sustained data transfer rate is

160 MByte/s per slot.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a

trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 245 MB/s on a PCI-X slot, up to 125 MB/s on a PCI slot and up to 160 MB/s on a PCIe slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

Singleshot output

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

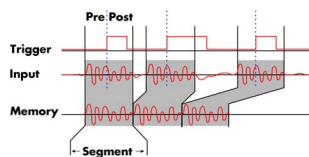
Repeated output

When the repeated output mode is used the data of the on-board memory is played continuously for a programmed number of times or until a stop command is executed. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

Single Restart replay

When this mode is activated the data of the on-board memory will be replayed once after each trigger event. The trigger source can be either the external TTL trigger or software trigger.

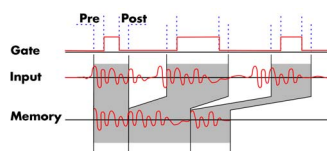
Multiple Recording



The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between.

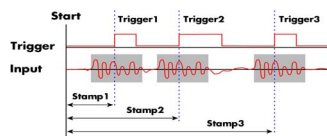
Gated Sampling



The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired.

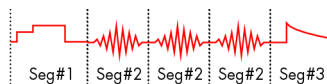
Timestamp



The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver.

Sequence Mode



The sequence mode allows to split the card memory into several data segments of different length. These data segments are

The sequence mode allows to split the card memory into several data segments of different length. These data segments are

chained up in a user chosen order using an additional sequence memory. In this sequence memory the number of loops for each segment can be programmed and trigger conditions can be defined to proceed from segment to segment. Using the sequence mode it is also possible to switch between replay waveforms by a simple software command or to redefine waveform data for segments simultaneously while other segments are being replayed.

Pattern trigger

For every bit of the digital input the pattern trigger defines individually the expected level or sets the bit to „don't care". In combination with pulsewidth counter and edge detection the pattern trigger could be used to recognise a huge variety of trigger events.

External trigger I/O

All digital boards can be triggered using an additional external TTL signal per acquisition module. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognized trigger event can - when activated by software - be routed to the trigger output connector to start external instruments.

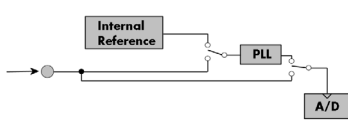
Pulse width

Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

External clock I/O

Using a dedicated line a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronize external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

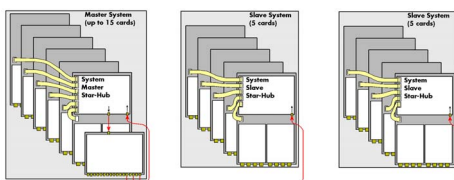
Star-Hub



The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards in one system. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and

clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The star-hub is available as 5 card and 16 card version. The 5 card version doesn't need an extra slot.

271 synchronous cards with the System Star-Hub



With the help of multiple system star-hubs it is possible to link up to 17 system phase synchronous with each oth-

er. Each system can then contain up to 16 cards (master only 15). In total 271 cards can be used fully synchronously in a bunch of systems. One master system distributes clock and trigger signal to all connected slave systems.

1-4 bits mode

On the model 7005 it is also possible to use just 1, 2 or 4 bits for acquisition or replay. In 1 bit mode the 8 times higher memory is then available, at 2 bits mode it is 4 times higher and at 4 bits mode it is double. This enlarges the recording/replay time in on-board memory and it reduces the transfer rate when using FIFO mode. The data is stacked internally to 8 bit samples. Therefore all information on memory/segment/pre and posttrigger sizes and steps can be up to 8 times higher.

BaseXIO (enhanced trigger)



The BaseXIO option offers 8 asynchronous digital I/O lines on the base card. The direction can be selected by software in groups of four. Two of these lines can also be used as additional external trigger sources. This allows the building of complex trigger conjunctions with external gated triggers as well as AND/OR conjunction of multiple external trigger sources like, for example, the picture and row synchronisation of video signals. In addition one of the I/O lines can be used as reference clock for the Timestamp counter.

Technical Data

Power Up

Data channels direction after power up
Clock and trigger output after power up

input (high impedance)
disabled

Digital Inputs

Direction	software programmable	all channels input or all channels output (no mixed direction)
Acquisition channel selection	software programmable	1, 2, 4, 8, 16, 32 or 64 (depending on card type)
Input Impedance	software programmable	110 Ω / 50 kΩ 15 pF
110 Ω termination voltage		2.5 V
Standard input levels		Low: ≤ 0.8 V High: ≥ 2.0 V
Absolute maximum Input levels		Low: ≤ -0.5 V High: ≤ 7.0 V
Data Input current sink	no termination	Low: -1.0μA (0.0 V) High: +1.0μA (3.3V), +20.0μA (5.0V)

Digital Outputs

Replay channel selection	software programmable	1, 2, 4, 8, 16, 32 or 64 (depending on card type)
Typical output levels	high impedance	Low: 0.2 V High: 2.8 V
Output max current load		Low: 64 mA High: -32 mA
Output levels at max load		Low: < 0.5 V High: > 2.0 V
Output Impedance (typical)		ca. 7 Ω
Stop level	software programmable	Tristate, Low, High, Hold Last

Output Delays

Trigger to 1st sample	≥ 8 active channels	19 clocks
Trigger to 1st sample	< 8 active channels	9 clocks + 10 * 8/active channels
Gate end to last replayed sample		19 samples (≥ 8 active channels)
Gate end alignment		[32 / active channels] in samples

Trigger

Running mode	software programmable	Singleshot, FIFO mode (Streaming), Multiple Recording, Multiple Replay, Gated Sampling, Gated Replay, Repeated Replay, Single Restart, Sequence Mode
Trigger modes	software programmable	Pattern and mask, edge, external TTL, software, pulsewidth, Or/And, Delay
Pattern and mask	software programmable	32 bit / 64 bit wide: 0 pattern, 1 pattern, don't care or edge
Trigger edge	software programmable	Rising edge, falling edge or both edges
Trigger pulse width	software programmable	0 to [64k - 1] samples in steps of 1 sample
Trigger delay	software programmable	0 to [64k - 1] samples in steps of 1 sample
Memory depth	software programmable	8 up to [installed memory / number of active channels] samples in steps of 4
Posttrigger	software programmable	4 up to [8G - 4] in steps of 4
Multiple Replay segment size	software programmable	8 up to [installed memory / 2 / active channels] samples in steps of 4
Multiple Replay, Gated Replay: re-arming time	≥ 8 channels	< 4 samples
Pretrigger at Multi, Gate, FIFO Recording	software programmable	8 up to [16352 Bytes / number of active channels] in steps of 8
Trigger output delay		19 clocks
Internal/External trigger accuracy	≥ 8 active channels	1 sample
Internal/External trigger accuracy	< 8 active channels	8/active channels samples (< 8 channels)
External trigger type (input and output)		3.3V LVTTTL compatible (5V tolerant)
External trigger input		Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 8 ns in pulse stretch mode, ≥ 2 clock periods all other modes
External trigger maximum voltage		-0.5 V up to +5.7 V (internally clamped to 5.0V, 100 mA max. clamping current)
Trigger impedance	software programmable	110 Ohm / high impedance (> 4 kΩ)
External trigger output levels		Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External trigger maximum voltage		-0.5 V up to +5.5 V
External trigger input current sink		± 1.0 μA (no termination)
External trigger output drive strength		Capable of driving 110 Ω and 50 Ω load

Clock

Clock Modes	software programmable	internal PLL, internal quartz, external. clock, external divided, external reference clock, sync
Internal clock range (PLL mode)	software programmable	1 kS/s to max using internal reference, 50kS/s to max using external reference clock
Internal clock accuracy		≤ 20 ppm
Internal clock setup granularity		≤ 1% of range (100M, 10M, 1M, 100k,...): Examples: range 1M to 10M: stepsize ≤ 100k
External reference clock range	software programmable	≥ 1.0 MHz and ≤ 125.0 MHz
External clock impedance	software programmable	110 Ω / high impedance (> 4 kΩ)
External clock range		DC up to max internal sample rate
External clock delay to internal clock		5.4 ns
External clock type/edge		3.3V LVTTTL compatible, rising edge used
External clock input		Low level ≤ 0.8 V, High level ≥ 2.0 V, duty cycle: 45% - 55%
External clock maximum voltage		-0.5 V up to +5.5 V (internally clamped to 5.0V, 100 mA max. clamping current)
External clock output levels		Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength		Capable of driving 110 Ω and 50 Ω load
External clock input current sink		± 1.0 μA (no termination)
Synchronization clock divider	software programmable	2 up to [8k - 2] in steps of 2

Sequence Replay Mode

Number of sequence steps	software programmable	1 up to 512 (sequence steps can be overloaded at runtime)
Number of memory segments	software programmable	2 up to 256 (segment data can be overloaded at runtime)
Loop Count	software programmable	1 to 1M loops
Sequence Step Commands	software programmable	Loop for #Loops, Next, Loop until Trigger, End Sequence
Special Commands	software programmable	Data Overload at runtime, sequence steps overload at runtime

BaseXIO Option

BaseXIO modes	software programmable	Asynch digital I/O, 2 additional trigger, timestamp reference clock, timestamp digital inputs
BaseXIO direction	software programmable	Each 4 lines can be programmed in direction
BaseXIO input		TTL compatible: Low ≤ 0.8 V, High ≥ 2.0 V
BaseXIO input impedance		4.7 kOhm towards 3.3 V
BaseXIO input maximum voltage		-0.5 V up to +5.5 V
BaseXIO output type		3.3 V LVTTL
BaseXIO output levels		TTL compatible: Low ≤ 0.4 V, High ≥ 2.4 V
BaseXIO output drive strength		32 mA maximum current, no 50 Ω loads

Connectors

Digital Inputs/Outputs	40 pole half pitch (Hirose FX2 series)	Cable-Type: Cab-d40-xx-xx
Option BaseXIO	8 x 3 mm SMB male on extra bracket, internally 8 x MMCX female	

Environmental and Physical Details

Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (Standard or with option star-hub 5)	1 full size slot
Width (star-hub 16)	additionally back of adjacent neighbour slots
Width (with option BaseXIO)	additionally extra bracket on neighbour slot
Width (with option -digin, -digout or -60xx-AmpMod)	additionally half length of adjacent neighbour slot
Weight (depending on version)	290g (smallest version) up to 460g (biggest version with all options, including star-hub)
Warm up time	10 minutes
Operating temperature	0°C to 50°C
Storage temperature	-10°C to 70°C
Humidity	10% to 90%

PCI/PCI-X specific details

PCI / PCI-X bus slot type	32 bit 33 MHz or 32 bit 66 MHz
PCI / PCI-X bus slot compatibility	32/64 bit, 33-133 MHz, 3,3 V and 5 V I/O

PCI Express specific details

PCIe slot type	x1 Generation 1
PCIe slot compatibility	x1/x4/x8/x16 (Some x16 PCIe slots are for graphic cards only and can not be used)

Certification, Compliance, Warranty

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark
Product warranty	2 years starting with the day of delivery
Software and firmware updates	Life-time, free of charge

Power Consumption

	PCI / PCI-X			PCI EXPRESS		
	3.3 V	5 V	Total	3.3V	12V	Total
M2i.7005/M2i.7010 (512 MB memory)	3.0 A	0.5 A	12.4 W	0.4 A	1.2 A	15.7 W
M2i.7011 (512 MB memory), 60 MS/s	3.2 A	0.5 A	13.4 W	0.4 A	1.1 A	14.5 W
M2i.7020 (512 MB memory), 125 MS/s	4.7 A	1.0 A	20.5 W	0.4 A	1.4 A	18.2 W
M2i.7021 (512 MB memory), 60 MS/s	5.4 A	0.9 A	22.7 W	0.4 A	1.3 A	17.0 W
M2i.7021 (4 GB memory), max. power	6.1 A	0.9 A	24.7 W	0.4 A	1.9 A	24.2 W

MTBF

MTBF	300000 hours
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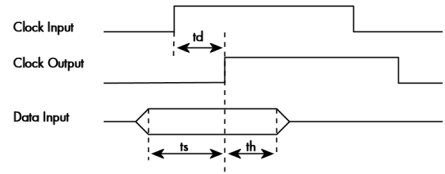
External clock-to-data timing

The setup and hold times as well as any delays relate to the output clock. If using external clock the timing depends on the used external range. Please be sure to meet this timing constraints if feeding in external clock.

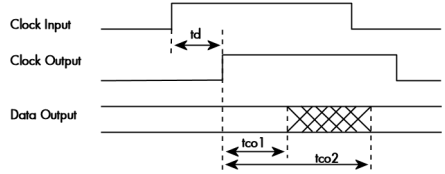
For detailed information on the different modes for external clocking please refer to the dedicated chapter in the hardware manual for the boards of the M2i.70xx series.

Input	Delay time	External Clocking Mode			Internal Clocking
		EXRANGE_LOW	EXRANGE_LOW_DPS	EXRANGE_HIGH	
	t_{id}	16.9 ns	1.6 ns	1.6 ns	n.a.
Data Output	t_{co1}	2.0 ns	2.0 ns	2.0 ns	2.0 ns
	t_{co2}	5.8 ns	5.8 ns	5.8 ns	5.8 ns
Data Input	t_s	2.1 ns	2.1 ns	2.1 ns	2.1 ns
	t_h	0.7 ns	0.7 ns	0.7 ns	0.7 ns
Trigger Output	t_{co1}	2.2 ns	2.2 ns	2.2 ns	2.2 ns
	t_{co2}	6.6 ns	6.6 ns	6.6 ns	6.6 ns
Trigger Input	t_s	1.5 ns	1.5 ns	1.5 ns	1.5 ns
	t_h	1.8 ns	1.8 ns	1.8 ns	1.8 ns

Input timing

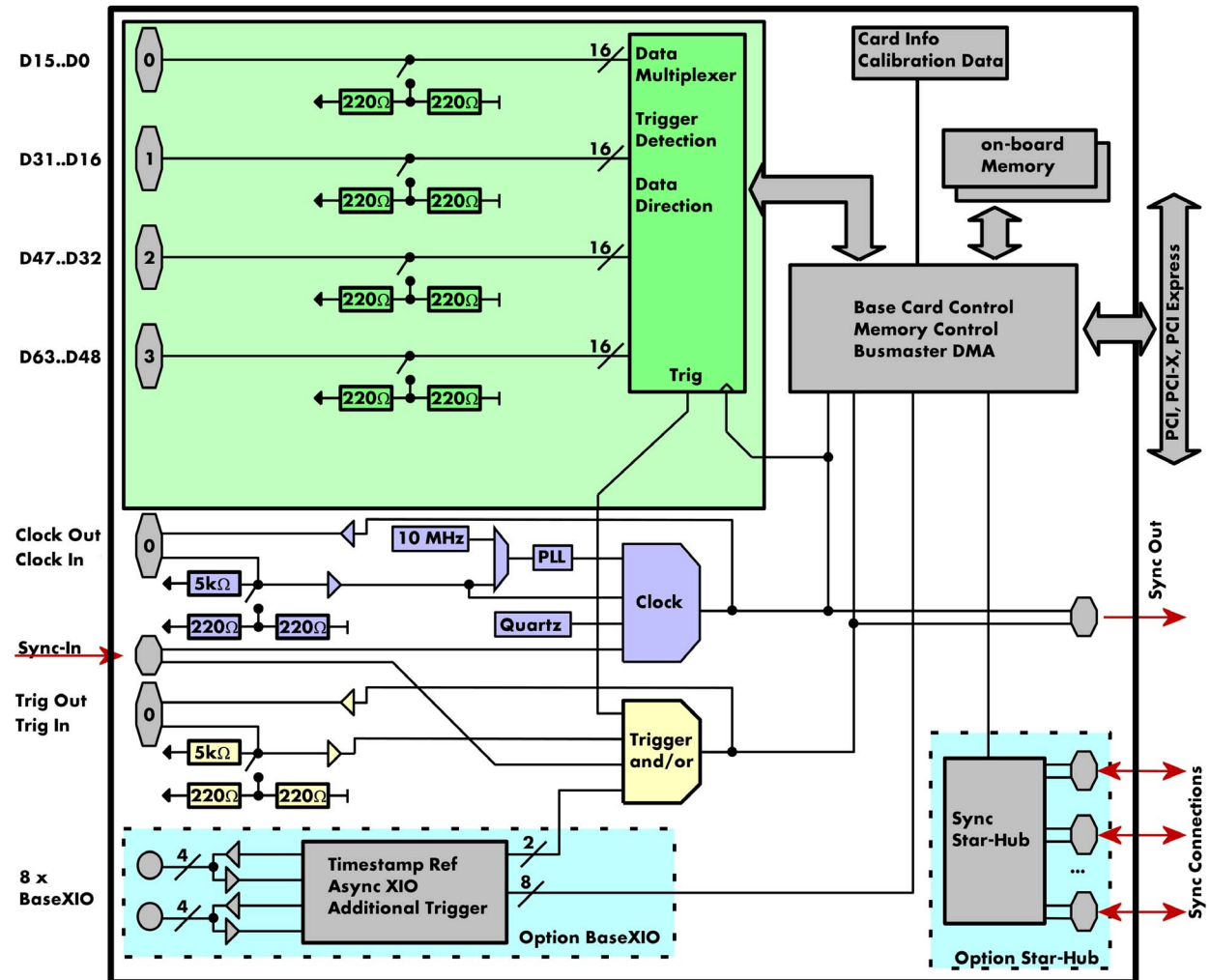


Output timing



When using external clock a delayed clock signal is generated on the Clock Output pin. The timing data in relation to this delayed clock output is similar to the timing when using internal clocking. It is therefore strongly recommended that you use the delay clock output for clocking any external devices.

Hardware block diagram



Order Information

The card is delivered with 512 MByte on-board memory and supports standard acquisition and replay (scope, single-shot, loop, single start), FIFO acquisition/replay (streaming), Multiple Recording/Replay, Gated Sampling/Replay, Timestamps and Sequence Mode. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows and Linux), LabWindows/CVI, .NET, Delphi, Visual Basic, Python and a Base license of the oscilloscope software SBench 6 are included. Drivers for other 3rd party products like VEE or DASyLab may be available on request.

One digital connecting cable Cab-d40-idx-100 is included in the delivery for every digital connection (each 16 channels).

PCI Express (PCIe)		PCI Express	PCI/PCI-X	Std Mem	1 Bit	2 Bit	4 Bit	8 Bit	16 Bit	32 Bit	64 Bit
PCI/PCI-X		M2i.7005-exp	M2i.7005	512 MB	125 MS/s	125 MS/s	125 MS/s	125 MS/s	125 MS/s		
		M2i.7010-exp	M2i.7010	512 MB	-	-	-	125 MS/s	125 MS/s		
		M2i.7011-exp	M2i.7011	512 MB	-	-	-	125 MS/s	125 MS/s	60 MS/s	
		M2i.7020-exp	M2i.7020	512 MB	-	-	-	125 MS/s	125 MS/s	125 MS/s	
		M2i.7021-exp	M2i.7021	512 MB	-	-	-	125 MS/s	125 MS/s	125 MS/s	60 MS/s

Memory	Order no.	Option
	M2i.xxxx-1GB	Memory upgrade to 1 GB of total memory
	M2i.xxxx-2GB	Memory upgrade to 2 GB of total memory

Options	Order no.	Option
	M2i.xxxx-SH5 (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
	M2i.xxxx-SH16 (1)	Synchronization Star-Hub for up to 16 cards
	M2i.xxxx-SSHM (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, PCI 32 Bit card, sync cables and extra bracket for clock and trigger distribution included
	M2i.xxxx-SSHMe (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, PCI Express card, sync cables and extra bracket for clock and trigger distribution included
	M2i.xxxx-SSHS5 (1)	System-Star-Hub Slave for 5 cards in one system, one slot width all sync cables + bracket included
	M2i.xxxx-SSHS16 (1)	System-Star-Hub Slave for 16 cards in system, two slots width, all sync cables + bracket included
	M2i.xxxx-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O and additional external trigger lines, additional bracket with 8 SMB connectors
	M2i-upgrade	Upgrade for M2i.xxxx: later installation of option -dig, -2DigM, -4DigM, -SH5, -SH16 or -bxio

Cables	for Connections	Length	Order no.	to BNC male	to BNC female	to SMA male	to SMA female	to SMB female
	BaseXIO line	80 cm		Cab-3f-9m-80	Cab-3f-9f-80	Cab-3f-3mA-80	Cab-3f-3fA-80	Cab-3f-3f-80
	BaseXIO line	200 cm		Cab-3f-9m-200	Cab-3f-9f-200	Cab-3f-3mA-200	Cab-3f-3fA-200	Cab-3f-3f-200
				to 2x20 pole IDC	to 40 pole FX2			
	Digital signals	100 cm		Cab-d40-idx-100	Cab-d40-d40-100			

Software SBench6	Order no.	Option
	SBench6	Base version included in delivery. Supports standard mode for one card.
	SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
	SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
	Volume Licenses	Please ask Spectrum for details.

(1) : Just one of the options can be installed on a card at a time.

(2) : Third party product with warranty differing from our export conditions. No volume rebate possible.

Technical changes and printing errors possible

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